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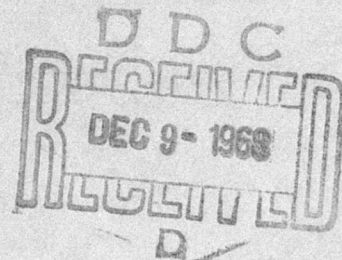| AUTHORITY |
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RADC-TR- 68-245
Final Report

ULTRASONIC FACE BOND RELIABILITY STUDY

A. G. Gross, Jr.
B. T. Hogan
N. F. Scudder
et al

Autonetics Division of North American Rockwell Corporation

TECHNICAL REPORT NO. RADC-TR-68-245
October 1968

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FOREWORD

This report was prepared by Autonetics, a Division of North American Rockwell Corporation, Anaheim, California, under RADC Contract F 30602-67-C-0083, Project 5519, Task 551904. The reporting period covered was November 1966 to June 1968. The RADC project engineer was John E. McCormick (EMERM).

The work was under the overall direction of Mr. A. G. Gross, Jr. The Principal Investigator for Phase I was Mr. B. T. Hogan; for Phase II, Mr. Hogan, and Mr. N. F. Scudder; and for Phase III, Mr. Hogan, Mr. A. M. Kinan, and Mr. W. A. Schmoyer.

This document does not contain classified information or extractions from classified documents.

Permission has been obtained to use copyrighted material in Appendix I, "Electrograph Method for Locating Pinholes in Thin Silicon Dioxide Films," previously published in The Journal of the Electrochemical Society, Vol 114, No. 6, pp 643-645, June 1967.

This report has been assigned Autonetics Division of North American Rockwell Corporation, Publication No. C7-850.2/501.

Distribution of this document is limited because it contains unclassified, specialized test data of interest only to Government agencies or Government contractors.

This technical report has been reviewed and is approved.

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ABSTRACT

Phase I of this program was concerned with the effect of ultrasonic bonding energy on the oxide coating of integrated circuit chips. The results indicate that a low level of oxide defects is caused by ultrasonic face bonding.

Phase II was to experimentally determine the optimum face-bonded assembly design. The "practical best" design was that which used a biaxial bonding pattern, a 7059 glass substrate, and aluminum projections with an as-bonded height of 2 to 3 x 10^{-4} inches.

Phase III was to fabricate and test a number of the "practical best" assemblies. The results showed (1) there was little or no effect due to thermally-induced mechanical strain, and (2) electrical continuity was maintained throughout twenty thermal cycles.

INTRODUCTION AND SUMMARY

The registrative interconnection concept, sometimes referred to as a "flip-chip" or (and herein) "face" bonding, consists of inverting unpackaged devices and bonding the metallized pads on the device to projections on a planar interconnection substrate (planar circuit). Variations of this are common. The projections may be on the device. Thermal-compression bonding or solder bonding may be used as well as ultrasonic bonding.

The concept permits improved miniaturization by eliminating individual device packages. The need for "fan out" patterns at each device is reduced. The number of bonds is reduced to one-half those required in conventional hybrid or "flying-lead" interconnection concepts. The bonding is rigid as each bond is a short column joining the device to the planar circuit. All bonds are made simultaneously (instead of sequentially) which affects a significant cost avoidance.

Disadvantages and uncertainties are also associated with face bonding. Heat transfer from the solid-state device to the planar circuit must occur primarily through the bonded projections which may not be located strategically for this purpose. Registration of pads with projections introduces an alignment problem involving very small dimensions. Inspectablility is uncertain. The effects of bonding energy on device reliability are unknown. The effects of face-bonded configuration and assembly design on functionality in varying environments are unknown.

The object of Phase I of this program was to determine the effect of several levels of ultrasonic bonding energy on the incidence of oxide defects in array type integrated circuit chips. A series of combinations of ultrasonic bonding energies and clamping forces were checked for their effects on oxide defects using an electrochemical autographic technique to measure defects in the silicon oxide. The results indicate that a low level of oxide defects is created by ultrasonic face bonding.

The object of Phase II was to experimentally determine the optimum face-bonded assembly design. Sixteen designs were investigated. Design variations were produced by using various combinations of planar circuit substrate material, bond material, bond size, and bonding pattern. Thermal strain on the silicon bars was measured during temperature cycling between -50 and +175C. Electrical continuity was measured before and after temperature cycling. Post-cycling metallographic analyses were performed also. The most practical design employed a biaxial bonding pattern, a 7059 glass substrate and aluminum projections with an as-bonded column height of 2 to 3 x 10^{-4} inch.

The objective of Phase III was to fabricate a number of the "practical-best" face-bonded assembly design as set forth in Phase II and to determine how they were affected by thermally-induced mechanical strain. Initially the assemblies were subjected to a single thermal cycle, during which the electrical parameters were monitored. Subsequently they were subjected to twenty thermal cycles, during which the electrical continuity of the bonds was monitored. After various stages of testing some of the face-bonds were metallographically sectioned. The test results indicated that the electrical parameters were relatively unaffected by the thermally-induced mechanical strain and that electrical continuity was maintained throughout the twenty thermal cycles.

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EVALUATION

Phase One of this program investigated the effect of ultrasonic energy used in the face bonding mode on the oxide coating that covers an integrated circuit. It was found that an increase in total defects in the oxide layer on the silicon chips and wafers that could be attributed to the ultrasonic energy was less than 20% of the total number of defects initially noted in the oxide layer.

Phases Two and Three developed and evaluated techniques for measuring mechanical stresses at the bond sites caused by thermal coefficient of expansion mismatches between the silicon chip and the substrate. The overall results indicate that thermally induced mechanical strain does not cause bond failure, even after repeated thermal cycling. However, extreme mismatches in substrate materials properties (specifically, coefficient of thermal expansion) is avoided.

The findings of Phase One confirm the results of a previous RADC effort, Contract AF30(602)-3921, in this technical area. The effects of ultrasonic energy on the silicon chip is neglible. The low level of oxide pinholes caused by ultrasonics is the only induced defect of any type that has been detected in this and the previous contractual efforts. (No device failures have been attributed to oxide defects in either effort.)

The findings of Phases Two and Three of this effort are gratifying and are a further indication of the work of ultrasonic face bonding. The technique has been proven to be a reliable and inexpensive method for assembling integrated circuits. It is recommended for use in U.S. Air Force electronic equipment.

JOHN E. McCORMICK
Solid State Applications Section
Reliability Branch

PHASE I

EXPERIMENTAL PROCEDURE

1. PREPARATION OF SILICON DICE

Silicon wafers measuring approximately 1.25 inches in diameter by 0.0032 to 0.0092 inch thick were procured from Texas Instruments, Inc. These wafers were doped with phosphorous and had resistivities in the range of 6 to 10 ohm-cm. An oxide layer of about 4000 anstroms thickness was generated at Autonetics on the surfaces of these wafers by means of a steam oxidation technique. Following steam oxidation, the wafers were treated such that P_2O_5 was diffused into the oxide layer. The P_2O_5 diffusion treatment was included to simulate electrically active circuits as closely as possible (the oxide layer on active devices would receive this treatment during the fabrication of emitter regions).

A photomask, illustrated in the upper portion of Figure 1, was generated to facilitate etching a 10-by-10 array of 0.060-inch by 0.080-inch rectangles in the oxide layer. The photomask include also, in the center of each rectangle, an identifying symbol.

The photomask pattern was etched through the oxide layer on one side of each wafer so as to expose bare silicon; at the same time the oxide was removed completely from the reverse side of each wafer. The etched lines which formed the array of rectangles were approximately 0.004 inch wide. The lower portion of Figure 1 shows an etched wafer.

In order to assess the significance of normal handling with respect to the introduction of defects in the oxide layer, four etched wafers were subjected to an ultrasonic-agitation treatment. These wafers were electrographed[1], agitated ultrasonically in a distilled water bath and electrographed again. Agitation was induced with a Sonogen Ultrasonic Generator, Model AP-25, at a setting of 90 milliamperes. Care was taken to ensure that none of the wafers contacted the walls of the bath container. The defect pattern in the oxide layers was not altered significantly by the agitation treatment. From these determinations it was concluded that normal handling would not jeopardize the validity of the experiment.

Another group of four oxidized and etched wafers were electrographed to characterize the pre-bonding defect pattern in each serialized rectangle. These electrographs were set aside for future comparison with electrographs made to characterize the post-bonding defect pattern.

Aluminum was vapor-deposited on the oxidized surface of each of the four wafers. This was accomplished in vacuum using an electron beam technique to vaporize the aluminum. The thickness of the vapor-deposited aluminum was determined to be approximately 8800 angstroms by an interferometric technique.

The aluminum coated wafers were then scribed along each of the lines which had been etched through the silicon oxide layer. After scribing, the wafers were diced. Through examination with a stereomicroscope it was determined that all breaking during dicing had occurred along the scribed lines and was within the 0.004-inch wide etched lines. No peeling of the aluminum coating was detected.

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[1]J. P. McCloskey, "Electrograph Method for Locating Pinholes in Thin Silicon Dioxide Films," J. of the Electrochemical Society, Vol 114, No. 6, June 67 Autonetics Publication X6-2914/501, dated 1 May 1967. See Appendix I.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
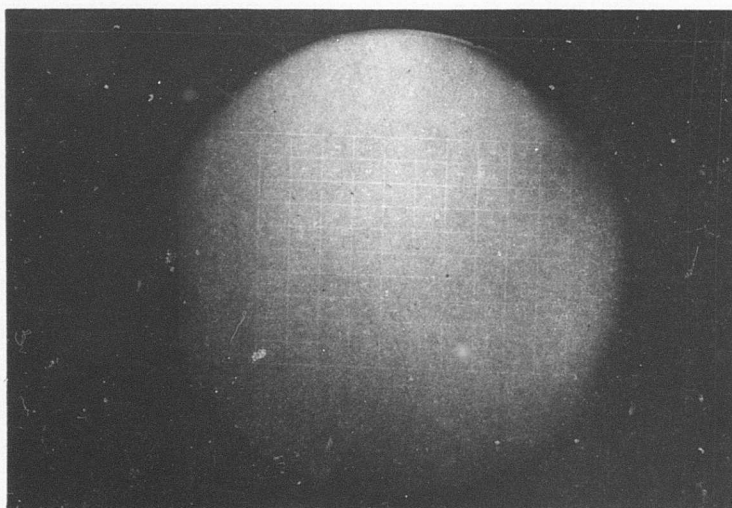
Figure 1. Die Boundary and Identification Pattern, and Etched
Silicon Oxide on a Wafer

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The dice from one of the four wafers were used for the effort described in Paragraph 3. The dice from the other three wafers were used for the effort described in Paragraph 4.

2. PREPARATION OF SIMULATED PLANAR CIRCUITS

Aluminum was vapor-deposited to a thickness of approximately 8000 angstroms on glass slides. A bonding pattern was produced on the glass slides by photomasking per Figure 2 and etching. Aluminum cones (bumps) were bonded to the pads. The cones were approximately 0.004-inch diameter at the base and were approximately 0.001 inch high. Bonding of the cones to the pads was accomplished with a Hughes Model 2901 machine.

3. ESTABLISHMENT OF FACE-BONDING PARAMETERS

In order to assure that only highly significant parameters would be employed in the principal experiment, a range of machine settings were investigated to identify the limits of a range which would:

1. Enclose a wide range of clamping forces and energy levels

2. Produce a bond shear strength of 200 grams or greater

From previous Autonetics' experience it was the consensus of engineering judgement that, when using the equipment described in Table I and Figure 3, machine settings of 1,100-gram clamping force and 1-second duration would be optimum for the system at hand. Thus, this auxiliary effort centered on these settings which produced the shear strengths presented in Table II. Table III presents the schedule of bonding parameters which were chosen for use in the principal experiment. All of these levels produced the required 200-gram minimum shear strength which was determined as depicted in Figure 4.
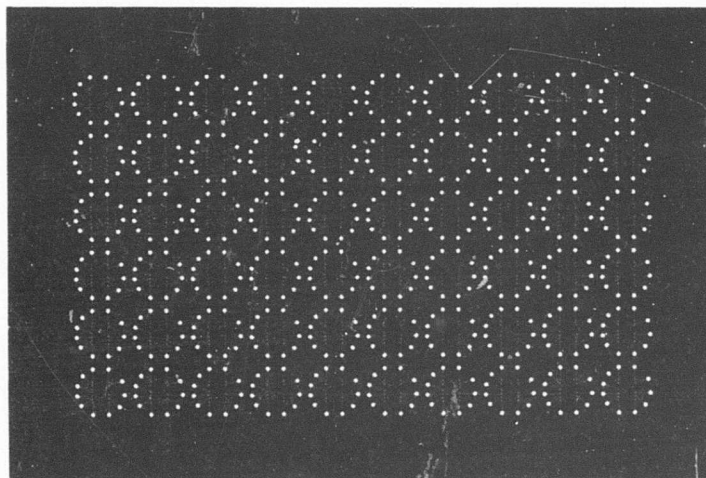
Figure 2. Bonding Pattern for Simulated Planar Circuits

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Table I. Face Bonding Equipment Description

A. Ultrasonic Power Supply:

- Gulton 224
- 36.7 kilocycles
- Constant output to transducer of 10 watts.

B. Timing Circuit:

- Lektra Lab TM-5

C. Transducer Tip:

- High carbon steel
- 0.100 inch diameter with a 0.020-inch diameter hole centered in the tip.
- Overall length: 31/32 inch
- Face to bottom of transducer: 0.36 inch
- Face polished with 4/0 emery paper prior to each use (each die).

Table II. Shear Strength for Dice Face-Bonded Using 1,100 Grams and 1 Second[1]

Die No.	Shear Strength (Grams)
1	580
2	580
3	700
4	580
5	480
6	570
7	540
8	410
9	590
10	380
Avg	541

1. Equipment as described in Table I
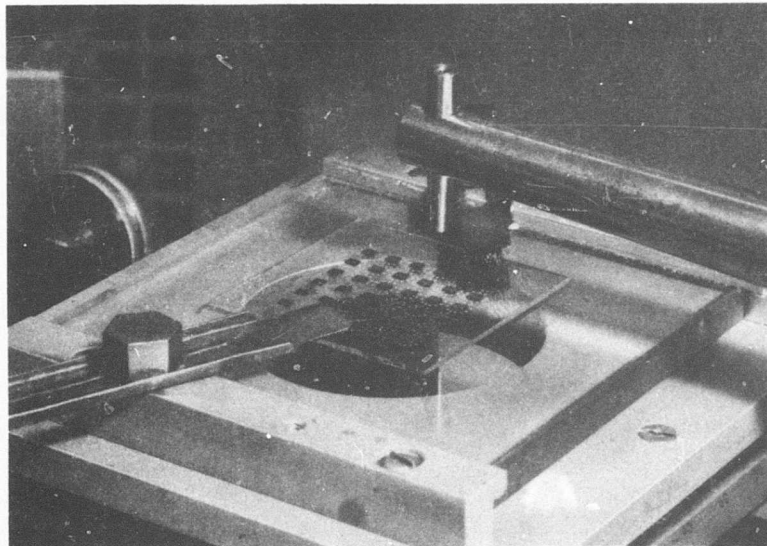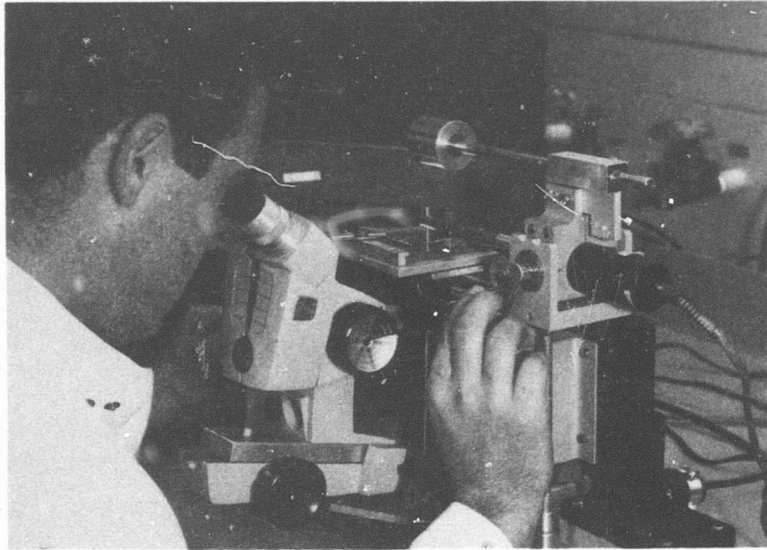
Figure 3. Ultrasonic Face-Down Bonding Equipment

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Table III. Schedule of Levels of Face-Bonding Parameters[1]

Level Identify	Clamping Force (Grams)	Time Duration (Seconds)	Energy Input[2] (Joules)
I	1100	0.2	2
II	1100	1.0	10
III	1100	5.0	50
IV	700	0.2	2
V	700	1.0	10
VI	700	5.0	50
VII	1500	0.2	2
VIII	1500	1.0	10
IX	1500	5.0	50

1. Using the equipment described in Table I
2. Input to the transducer
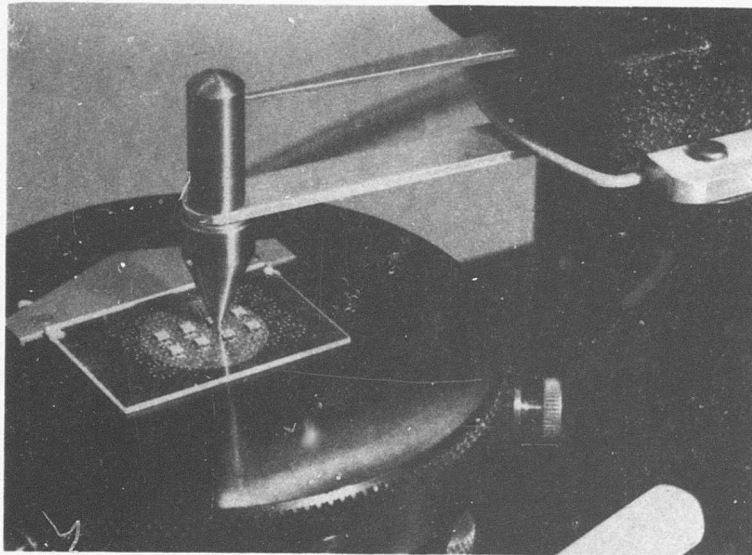
Figure 4. Shear Test Equipment Used to Determine the Strength of Face-Bonded Dice

4. FACE BONDING AND DISMOUNTING OF DICE

One simulated planar circuit was used as a mounting platform for each of nine sets of six dice. For a given platform, all six dice were mounted at a unique combination of machine settings. Also for a given platform, the six dice were selected such that two had originated in each of three different wafers. The 54 dice were face-down bonded to the nine simulated planar circuits in accordance with the schedule presented in Table III.

During the bonding operation the operator noted that some of the dice fractured. After bonding, a thorough microscopic inspection was performed on each of the 54 dice. This examination revealed a number of defective dice as described in Table IV. Many of the remaining dice exhibited abrasions on the surface contacted by the transducer tip; this effect is illustrated in Figure 5.

The two chipped dice noted in Table IV were not replaced. The eight broken dice noted in Table IV were replaced. These eight dice were all mounted on a unique simulated planar circuit, using for each die the bonding parameters appropriate to it as shown in Table IV. These face-bonding operations differed from the initial operations in that resonance was detuned by changing the voltage from 6.5 to 8.0 volts. No breakage was noted as a result of these operations.

The 54 dice were dismounted from the simulated planar circuits by dissolving all of the aluminum, vapor-deposited films and cones, with 12-normal hydrochloric acid. This operation not only dismounted the dice but prepared them for terminal electrographic characterization as well.

Table IV. Dice Fractured During Face Bonding[1]

Incidence No.	Fracture Character	Clamping Force (Grams)	Duration Time (Seconds)	Energy Input[2] (Joules)
1	Chipped Edge	700	1.0	10
2	Chipped Edge	1500	1.0	10
3	Broken in half	700	1.0	10
4	Broken in half	700	5.0	50
5	Broken in half	700	5.0	50
6	Broken in half	700	5.0	50
7	Broken in half	1100	0.2	2
8	Broken in half	1500	0.2	2
9	Broken in half	1500	5.0	50
10	Broken in half	1500	5.0	50

1. Using equipment described in Table I

2. Input to the transducer
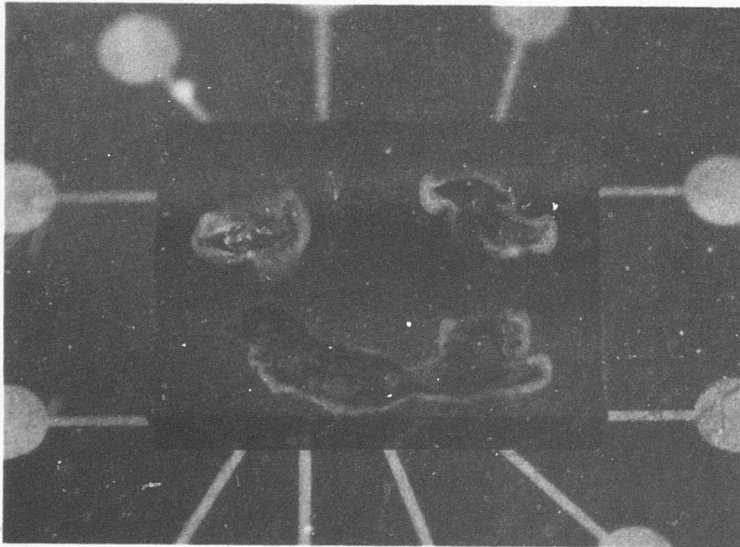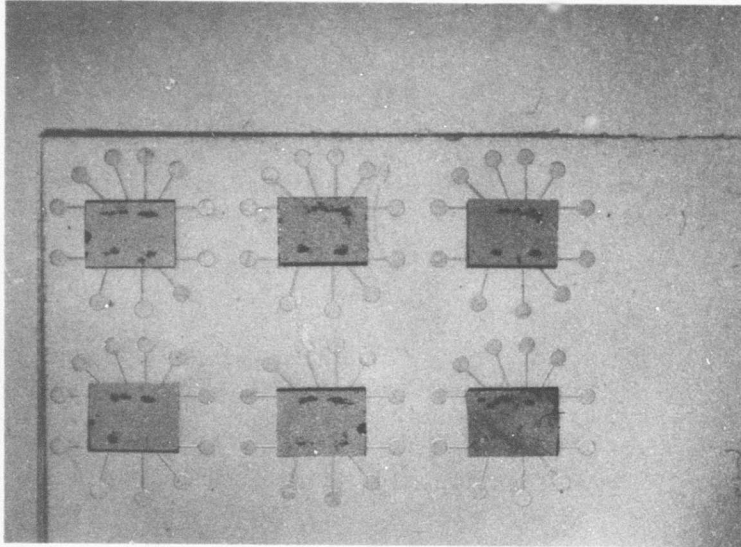
Figure 5. Abrasion of Silicon Dice by Transducer Tip

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5. POST-BONDING CHARACTERIZATION OF DICE

An electrograph was produced for each of the 54 dice. It was necessary to develop special tooling for this process since the size disparity between wafers and dice was so great. However, the essential features of the electrographic process were not altered.

6. EVALUATION AND VERIFICATION OF ELECTROGRAPHS

All electrographs were examined thoroughly at 120X magnification. At least two, and often three, replications were made for each specimen. It was required that the same characterization be produced by two successive electrographs before it was accepted as valid.

RESULTS

Table V presents the results of the electrographic characterizations. Figure 6 illustrates some typical indications on electrographs.

The results presented in Table V suggest, but do not demonstrate unambigously, that the ultrasonic face-bonding operation does not introduce new defects in silicon dioxide film on dice. The suggestion stems principally from the fact that the frequency of occurrence of new defects was not systematic with variations in bonding parameters. Further, in half of the instances, the new defects were not close to the sites of bonds.

On the other hand it may be argued with equal vigor that all levels of bonding parameters were sufficiently intense to introduce oxide defects at some low frequency of occurrence. This latter argument is bolstered substantially by the relatively random occurrence of die breakage during bonding which was noted in Table IV. Indeed, if virtually all of the bonding conditions were severe enough to fracture dice at some low frequency of occurrence then it does no seem unreasonable to conclude that virtually all of the bonding conditions were severe enough to induce defects in the oxide layer at some low frequency of occurrence. The facts that 10 of 54 dice fractured during bonding and that 10 of 54 unfractured dice had new defects introduced during processing, may not be a statistically significant parallel due to the limited amount of data but this numerical similarity is highly suggestive.

The principal fact which thwarts unambiguous interpretation of the data is that the "before" characterizations were produced before vapor deposition of aluminum, scribing, dicing, and face-bonding. The possibility exists that new defects (detected after bonding) were introduced at any or all of these steps. An auxiliary experiment would be required to assess the plausibility of assigning some or all of the new defects to process steps other than face-bonding.

An experiment was conducted to isolate the cause of the change in number of defects noted in Table V. A new set of samples was electrographed before and after vapor deposition of aluminum, scribing, and dicing. The results of this effort follow.

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Table V. Results of Electrographic Characterization

No. of Dice	Bonding Parameters			No. of Defects Detected		Proximity of New Defects to Bond Pads[1]
	Force (grams)	Time (seconds)	Energy (joules)	Before (in wafer)	After (on dice)	
4	700	0.2	2	0	0	N.A.[2]
2	700	0.2	2	0	1	not close
6	700	1.0	10	0	0	N.A.
5	700	5.0	50	0	0	N.A
1	700	5.0	50	0	1	not close
4	1100	0.2	2	0	0	N.A.
1	1100	0.2	2	0	1	close
1	1100	0.2	2	0	1	very close
5	1100	1.0	10	0	0	N.A.
1	1100	1.0	10	0	1	not close
5	1100	5.0	50	0	0	N.A.
1	1100	5.0	50	0	1	very close
5	1500	0.2	2	0	0	N.A.
1	1500	0.2	2	2	2	N.A.
4	1500	1.0	10	0	0	N.A.
1	1500	1.0	10	0	1	not close
1	1500	1.0	10	0	1	very close
5	1500	5.0	50	0	0	N.A.
1	1500	5.0	50	1	2	not close

1. The precise locations of bonding pads could not be determined since all of the aluminum had been removed. Thus, an estimate of proximity is presented. New defects are those introduced by processing.

2. "N.A." means not applicable.

10
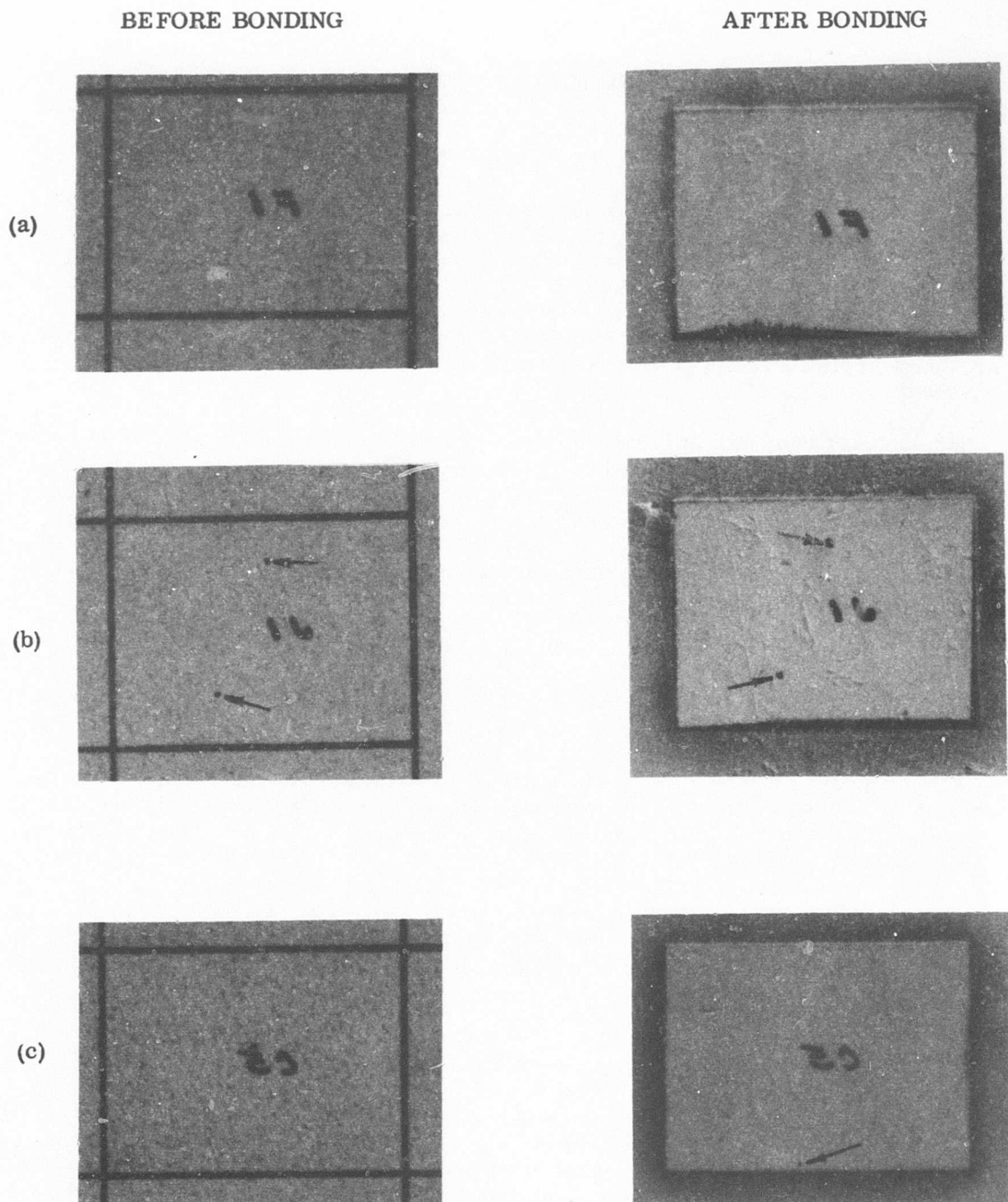
Figure 6. Typical Electrographs of Areas on Wafers Before Bonding
and After Bonding of Dice   (a) No oxide defects before or after
face bonding, (b) Two oxide defects both before and after face
bonding, and (c) No oxide defects before face bonding and one
defect after face bonding (Arrows indicate defect locations.)

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VERIFICATION OF RESULTS

INTRODUCTION:

This investigation was conducted to determine if ultrasonic face bonding introduction defects (pinholes) in the silicon dioxide of circuit dice. A previous investigation, indicated an increase in oxide defects, however, their cause could not be related specifically to face bonding. It is possible that the increase in defects could partially or completely be attributed to processing operations performed on the silicon wafers or dice before face bonding. This investigation is, therefore, directed at separating oxide defects caused by circuit die preparation from oxide defects caused by ultrasonic face bonding.

The results of this investigation are compared to the results obtained in the previous investigation to substantiate the validity of both test results.

CONCLUSIONS:

1. The results of this investigation indicate that a low level of oxide defects is created by ultrasonic face bonding.

2. The creation of oxide defects by wafer and die processing steps is insignificant.

3. The increase in oxide defects noted after face bonding occurred at a wide level of energies applied to the dice. This indicates that all levels of bonding energy may be sufficient to create oxide defects, that the ability of an oxide to be damaged varies depending upon the nature of each defect, or the defects might be caused by the bonding weight and subsequent load distribution on the die.

4. Defects were randomly dispersed on the die surface. Therefore, the ultrasonic energy must be distributed across the die during the bonding operation and not just in areas at, or adjacent to, the interconnection cones.

PROCEDURES AND RESULTS:

1. Six silicon wafers were selected for testing. Each wafer was steam oxidized to an oxide thickness of 4,000 Å. The oxidation was followed by a P_2O_5 diffusion of approximately 200 – 300 Å into the oxide. Each wafer was then subjected to a photomask and etching operation. The pattern etched into the oxide is illustrated in Figure 7. This etching operation simulates etching performed for fabrication of bipolar devices, indicates the die boundaries for each die to be taken from the wafer, and identifies each die.

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The oxide defect presence was then determined and recorded by preparing an electrograph of each of the six oxidized wafers. (Appendix I) This level of oxide defects was used as the reference point for comparison to defects found after processing and bonding, see Table VI.

2. All six wafers were then submitted for further preparation. The preparation again simulated processing that would occur if bipolar circuits were being fabricated. A continuous aluminum film was vacuum deposited on the surface of each wafer. Approximately 8,000 Å were deposited. The wafers were then scribed in the grid lines that were previously etched through the oxide. The wafers then were diced.

3. Three wafers of the group (numbers 29, 30 and 31) were selected for testing to determine the number of oxide defects after dice preparation. To determine the occurrence of defects, a number of dice were selected from each wafer. An electrograph was made of each of these dice. The aluminum metallization on the die surface had to be removed before the electro-graphing process. This was accomplished by etching with HCl. The number of defects were counted. The defects noted were compared to the number of defects found (in each die under test) in the wafer at the reference level of testing. A total of 26 dice was examined. Only one oxide defect was found in the dice that was not observed in the reference level. This indicates that processing (vacuum deposition, scribing, and dicing) insignif-icantly affects the oxide.

4. Dice were then selected from each of the three remaining wafers (numbers 32, 33 and 34) for further testing. These dice were face bonded. The material combinations and bonding parameters were as listed in Table VII. The bond schedules used were the same as used in a previous test.

After face bonding, each die was removed from its substrate by dissolving all aluminum with HCl. Thus, the dice were removed from the substrates without additional stressing and were ready for electrographing.

Each face bonded die was electrographed. The number of oxide defects was counted. The results were compared to the reference level to determine if face bonding caused oxide defects. The results were also compared to the energy level applied to the die during the face bonding operation to see if any correlation existed. An increase of seven defects was observed. The occurrence of the increase of defects could not be related to any particular level of bonding energy, see Table VII.

5. The defects that were found after bonding, but not in the reference level samples, were examined to determine their proximity to the interconnection cones. Four of the defects were possibly at the interconnection cone loca-tion, and the remaining three were not.

Table VI. Occurrence of Oxide Defects in Test Wafers at Reference Level*

| Wafer 29 | | Wafer 30 | | Wafer 31 | | Wafer 32 | | Wafer 33 | | Wafer 34 | |
Die	Defects	Die	Defects	Die	Defects	Die	Defects	Die	Defects	Die	Defects
A2	3	A10	0	A7	0	A9	0	B9	0	A10	0
B10	0	B8	0	D3	0	J8	0	B10	0	C3	0
D10	0	D7	0	E1	1	G7	0	C1	0	H4	0
E3	0	E4	0	E2	0	G10	0	G8	0	J2	0
E8	0	E5	0	F1	0	D3	0	A8	0	J10	1
F6	0	F3	0	G3	0	J6	0	K6	0	B2	2
F8	1	G5	1	G8	0	K10	2	A3	1	E1	2
D8	1	H1	2	H3	0	H1	1	H10	1	K7	2
				J7	0	B5	1	D4	2	K10	3
				K7	0	J1	1				

* Only dice that were later used in the testing are listed.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
H1	H2	H3	H4	II5	H6	H7	H8	H9	H10
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10

Figure 7.   Photomask Pattern Etched Through
The Oxide of Each Silicon Wafer

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Table VII. Bond Schedules and Material Combination of Face Bonded Dice

Bond Schedule No.	Machine Settings	No. of Dice Face Bonded	Increase in Defects
1	1,100 grams; 0.2 sec.	3	1
2	1,100 grams; 1.0 sec.	4	1
3	1,100 grams; 5.0 sec.	3	0
4	700 grams; 0.2 sec.	3	0
5	700 grams; 1.0 sec.	4	0
6	700 grams; 5.0 sec.	3	3
7	1,500 grams; 0.2 sec.	3	1
8	1,500 grams; 1.0 sec.	4	1
9	1,500 grams; 5.0 sec.	3	0

Interconnection cones were bonded to the substrates.
Cone size was 0.004 inch base diameter and 0.002 inch height.
Dice were then registered on the interconnection cones and face bonded with the above parameters.

6. The results of this investigation were compared to the results of the previous investigation. A total increase of seven oxide defects after bonding were detected in this test, and a total of nine defects were found in the previous investigation. Hence, a repeatability was demonstrated.

7. In summary, an increase of only one defect was noted in the samples after dice preparation. In both investigations, an increase of defects was noted after bonding. The defects found (after bonding) were randomly scattered over the die surface - sometimes possibly at an interconnection cone location, and sometimes not. The occurrence of defects could not be related to any particular level of bonding energy.

DISCUSSION:

An oxide defect is, as determined by testing in this investigation, an area capable of conducting a one milliamp current when the sample is submerged in a benzidine in acid solution and is biased across the oxide itself. The voltage required to cause conduction of one milliamp was normally 5 to 10 volts. The ability to detect a defect depends upon the resolution of the microscope used to examine the electrographs. The minimum size defect observed in this investigation was approximately 5.0×10^{-5} inch in diameter.

The effect any oxide defect would have on an electrical circuit would depend upon the location of the defect with respect to devices and metallizations within the circuit. The dice tested for this program simulate double diffused, junction isolated, integrated circuits. The results of this investigation are limited to the type of oxide present on these test samples. The P_2O_5 diffusion into the oxide (approximately 200 to 300 Å) of these test samples affects the integrity of the oxide, **Reference (1)**. Devices fabricated by another technique may react differently than observed in this test resulting in a larger or smaller number of oxide defects.

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PHASE II

EXPERIMENTAL PROCEDURE

1. EXPERIMENTAL DESIGN

In order to explore the mechanical reliability of face-bonded assembly designs a matrix of input variables was established. The matrix was fully factorial and contained two levels on each of four independent variables. These independent variables were bonding pattern, planar circuit material, interconnection material, and interconnection (projection) size.

The levels on each of these variables were selected to produce substantial contrast in the output variables as well as to encompass the design limits currently contemplated in industry.

The bonding pattern levels were defined in terms of the nominal strain state which they would induce during temperature excursions: uniaxial and biaxial. These patterns are depicted in Figures 8 and 9.

The planar circuit materials were chosen to be transparent (to minimize alignment difficulties) and to provide a substantial difference in thermal expansion: soda-lime glass (microscope slide) and 7059 glass.

The two interconnection materials were those most often used to interconnect solid-state devices: gold and aluminum.

The interconnection heights were chosen to provide bonded column heights differing by at least a factor of two: 0.001 and 0.002 inch (prior to face bonding).

Table VIII summarizes the input-variable matrix which consists of sixteen cells. A minimum of five replications of each assembly design (experimental cell) were produced for use in the experiment.

In order to produce appreciable mechanical strain (inches/inch) the specimens were cycled between the temperature limits of approximately -50 and +200C. This cycling was replicated three times for precision.

A principal output variable was mechanical strain as a function of temperature excursion. Room temperature, 24 C, was taken as the standard state (zero strain reference). Strain was measured perpendicular to the bond lines of specimens from cell No. 9 through 16. This strain direction was parallel to the larger edge dimension of the die and was termed "longitudinal strain." Both longitudinal strain and transverse strain were measured on specimens from cell No. 1 through 8.

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*LOCATION OF
FACE-BONDED
SILICON BARS

*LOCATION OF
FACE-BONDED
SILICON BARS
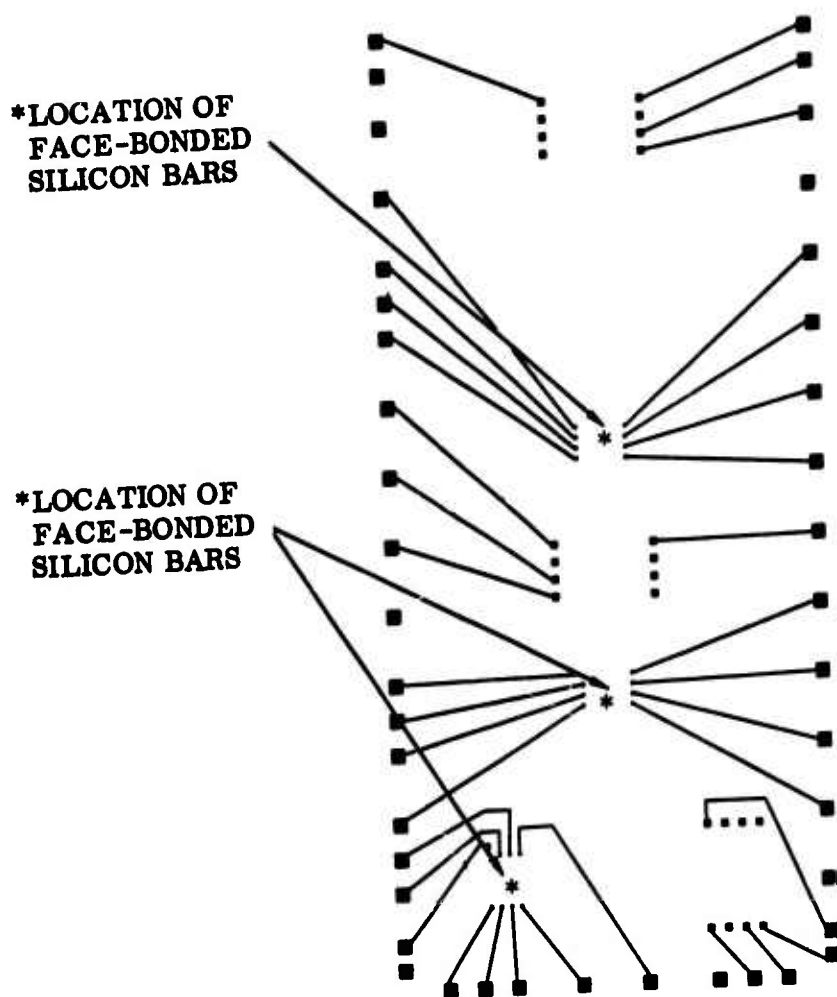
Figure 8.   Planar Circuit Metallization Pattern for Uniaxial Strain Condition

20
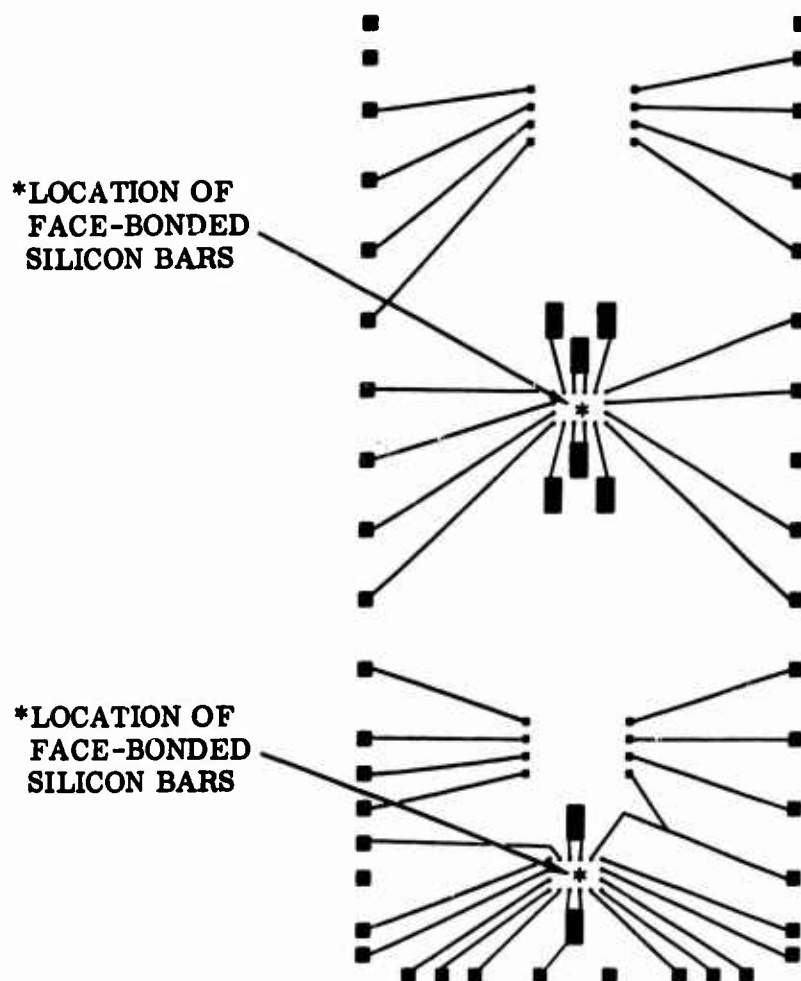
Figure 9. Planar Circuit Metallization Pattern for Biaxial Strain Condition

Table VIII. Assembly Designs for Face Bonded Specimens

Experimental Cell Number	Nominal Strain Condition	Planar Circuit Substrate Material	Interconnection Cone Material	Projection Cone Height (inches)
1	Biaxial	Soft Glass	Gold	0.001
2	Biaxial	Soft Glass	Gold	0.002
3	Biaxial	7059 Glass	Gold	0.001
4	Biaxial	7059 Glass	Gold	0.002
5	Biaxial	Soft Glass	Aluminum	0.001
6	Biaxial	Soft Glass	Aluminum	0.002
7	Biaxial	7059 Glass	Aluminum	0.001
8	Biaxial	7059 Glass	Aluminum	0.002
9	Uniaxial	Soft Glass	Gold	0.001
10	Uniaxial	Soft Glass	Gold	0.002
11	Uniaxial	7059 Glass	Gold	0.001
12	Uniaxial	7059 Glass	Gold	0.002
13	Uniaxial	Soft Glass	Aluminum	0.001
14	Uniaxial	Soft Glass	Aluminum	0.002
15	Uniaxial	7059 Glass	Aluminum	0.001
16	Uniaxial	7059 Glass	Aluminum	0.002

Another principal output variable was evaluation of the electrical integrity of the face bonds after thermal cycling.

Auxiliary output variables included visual examination of bond sites and metallographic examination of cross sections of bonds.

2. SPECIMEN PREPARATION

Planar circuits were designed to produce the uniaxial and biaxial strain conditions. The metallization pattern photomasks for the two conditions are shown in Figures 8 and 9 The planar circuit substrate for the uniaxial strain condition was designed to carry three face-bonded silicon bars and three (face-up) flying-lead bonded bars for temperature compensation. The planar circuit substrate for the biaxial strain condition was designed to carry two face-bonded bars and two temperature-compensating bars.

The planar circuit substrates measured 1.50 by 0.75 by 0.048±0.004 inches. Corning 7059 glass and Corning microscope slides (soda-lime glass) were used. One side of each substrate was coated first with a vacuum-deposited layer of nickel-chromium. The nickel-chromium layer was approximately 100 angstroms thick. Aluminum was subsequently vacuum deposited on the nickel-chromium to a thickness of approximately 8000 angstroms.

The vacuum-deposited films were tested for adhesion to the glass substrate and for bondability. An aluminum wire (1-percent silicon) measuring 0.001 inch in diameter was bonded ultrasonically to the film. A tensile load sufficient to cause fracture was then applied to the wire. Only when fracture occurred in the wire and outside the bond region was a film accepted for use in the program.

Acceptable metallized substrates were photomasked with Kodak Thin-Films Resist (KTFR) using the patterns in Figures 8 and 9. The aluminum was etched with a solution of methol alcohol and sodium hydroxide. The nickel-chromium was etched with a solution of cerric sulfate and nitric acid. The KTFR was then removed.

Photomasks were laid out so that silicon bars could be fabricated with five piezo-resistive elements diffused into an 0.080 x 0.100-inch bar.* This required the preparation of photomasks for resistor zones, window contacts, and aluminum metallization interconnects and loading pads. Figure 10 illustrates these patterns. The photomasks carried a 21 x 14 array of these patterns which fit on a 1-inch diameter, 0.010-inch thick wafer of (111) silicon.

The resistors were formed by boron diffusion. The desired resistance was 120 ohms.

The processed wafers with resistor contact windows and die boundary lines etched in the grown silicon oxide were metallized with a vacuum-deposited film of aluminum. The film thickness was approximately 8000 angstroms. The metallized wafers were photomasked and etched to produce the desired expanded contact pattern.

*(The purpose of these elements was to serve as anc'''ary strain-measuring devices)
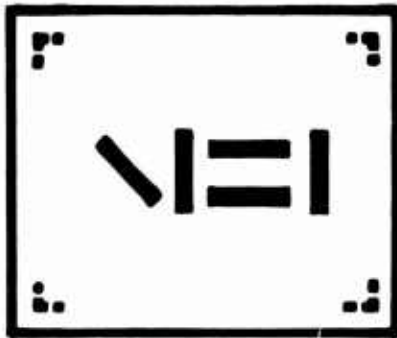
DIFFUSED RESISTOR PATTERN
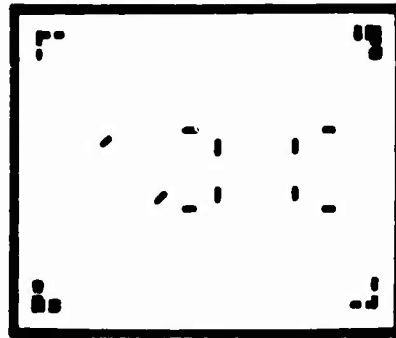
CONTACT WINDOW PATTERN
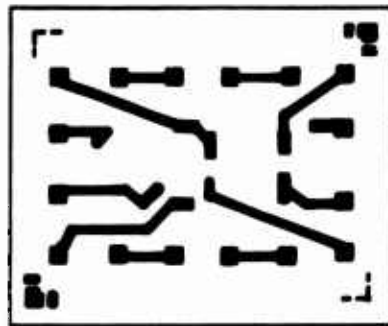
ALUMINUM METALLIZATION PATTERN

Figure 10. Photomask Patterns for Resistor Fabrication and
Interconnection of Silicon Bars

The aluminum on the resistor contact windows was alloyed with the resistor material at an elevated temperature. Figure 11 shows a wafer processed in this manner.

The wafers were subjected to resistance measurements in order to identify a homogeneous population of devices. Although the target resistance was 120 ohms, it was found that the largest population fell in the range of 83.0 ± 3.5 ohms. Silicon bars not included in this range were marked for rejection.

The wafers were then scribed and diced. Acceptable devices were segregated for use.

Conical projections were bonded ultrasonically to the metallized bond sites on the glass planar circuit substrates. Gold and aluminum cones of two sizes were mounted. The gold was 99.99-percent pure. The aluminum was alloy 1100. The larger cone size had a base diameter of 0.005 inch and was 0.002 inch high. The smaller cone size had a base diameter of 0.003 inch and was 0.001 inch high.

The aluminum cones were mounted using a clamping force of 100 grams. The larger cone size was bonded using 2.6 watts for 60 milliseconds. The smaller cone size was bonded using 0.6 watts for 60 milliseconds.

The gold cones were mounted using a clamping force of 130 grams. The larger cone size was bonded using 1.5 watts for 60 milliseconds. The smaller cone size was bonded using 0.95 watts for 60 milliseconds.

Figure 12 shows mounted projection cones.

After mounting projections on the planar circuits, the silicon bars were face bonded to the registered projections. This was accomplished using a Gulton, Glennite Ultrasonic Soldering Iron, Model US 10, modified to accept a variety of transducer tips. This unit provided a constant 10 watts at output frequencies between 32 and 42 kHz. The unit was equipped with a voltmeter across the output of the power supply to facilitate resonance adjustment.

The glass planar circuit substrates were clamped on the bonding stage as shown in Figure 13. The bar was then placed face down on the projections and was brought into registry. The transducer tip, preadjusted to be parallel to the back of the die, was then brought into contact with die at a predetermined load. Ultrasonic energy, 10 watts, was then applied for a predetermined time to form the bonds. Table IX presents the bonding schedule for each cell in Table VII.

Several criteria were used to establish the face-bonding schedule. The schedule had to produce a minimum shear load (on the bar) to failure of 200 grams, a face-bonded column height of 0.0002 to 0.0003 inch for small projections and of 0.0008 to 0.0010 inch for large projections, and electrical continuity in all resistor circuits. Figure 14 illustrates the shear testing apparatus. An optical comparator was used to measure column heights. Continuity was evaluated with an ohmmeter.

The bars used in the program, bonded according to Table IX, were inspected visually for mechanical damage and all circuits were inspected for electrical continuity. In each cell, several sacrificial dice were tested for shear strength to assure that the bonding schedule was producing the minimum 200-gram shear strength. Typically, all schedules produced shear strengths in the range of 500 to 700 grams.

25

5-17-67   700-72A-662 B
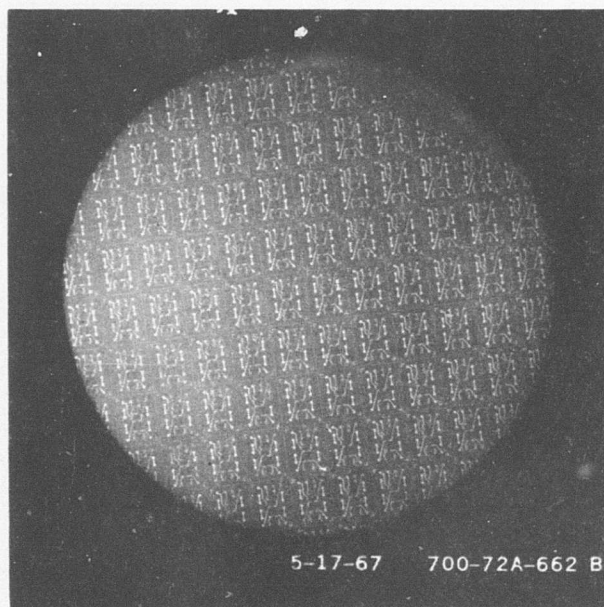
Figure 11. Silicon Wafer with Diffused
Resistors and Expanded Contacts

26
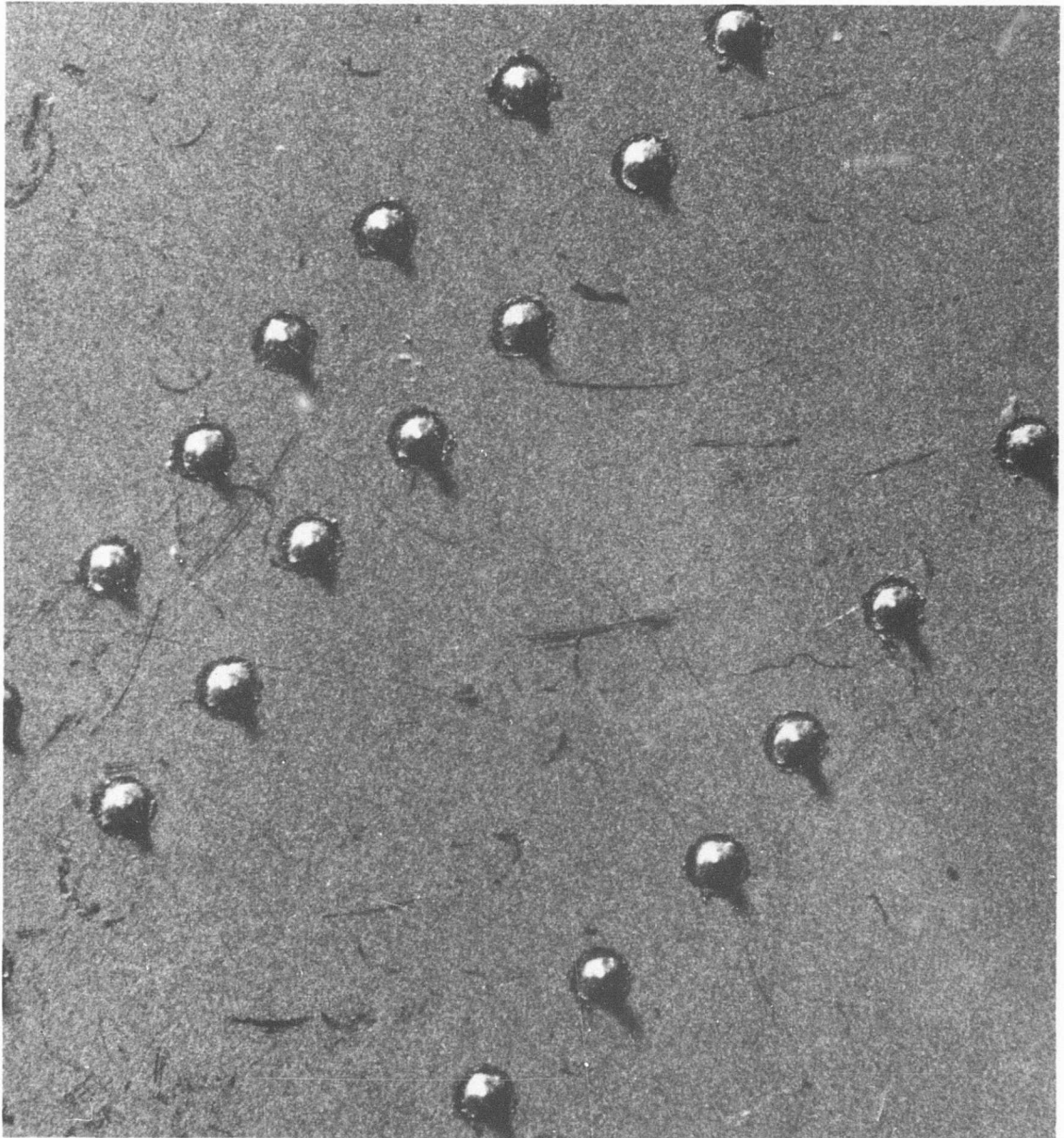
Figure 12. Interconnection Projections (Cones)
on Unetched Aluminum Metallization
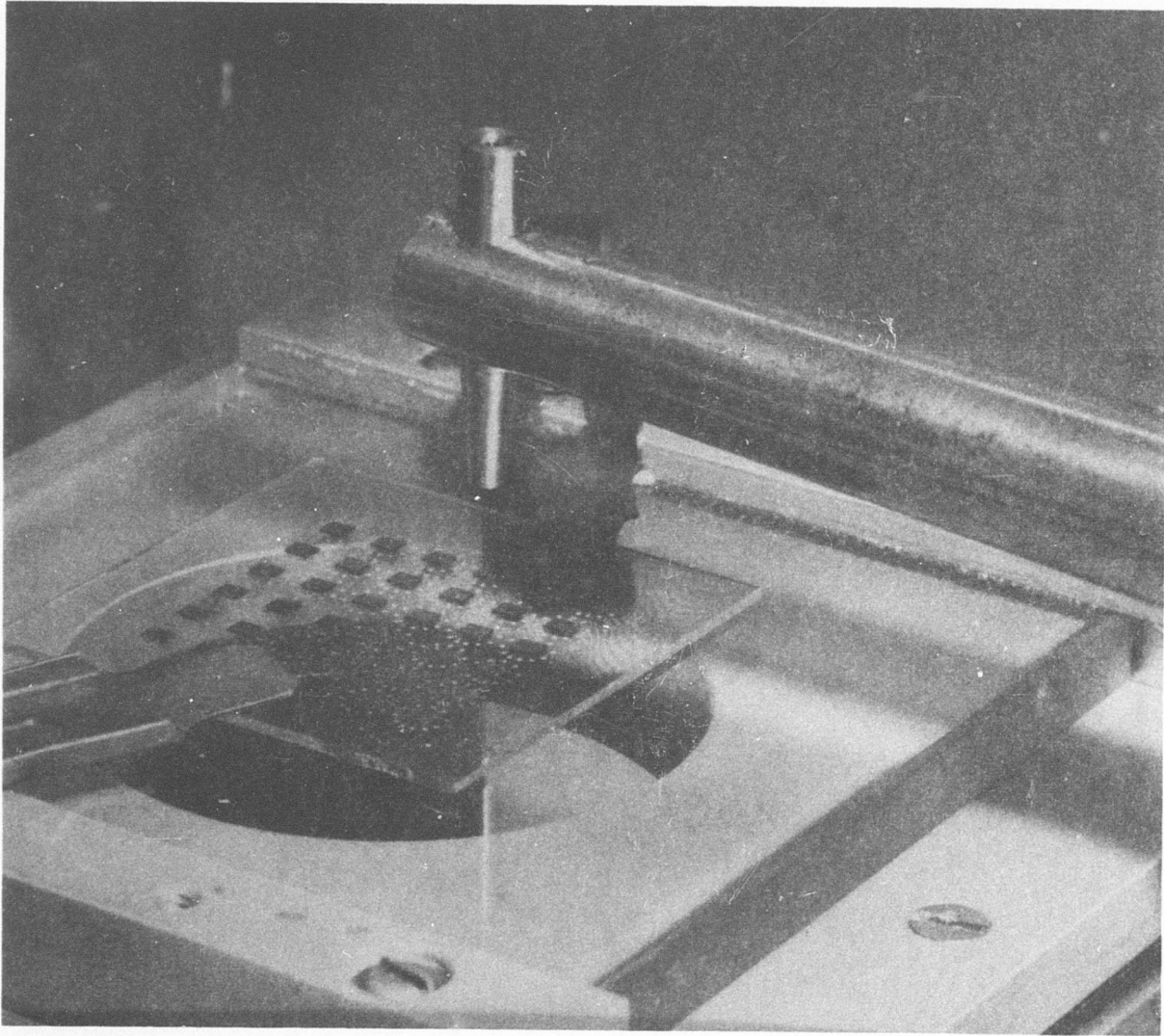
Figure 13.   Ultrasonic Face-Bonding Equipment
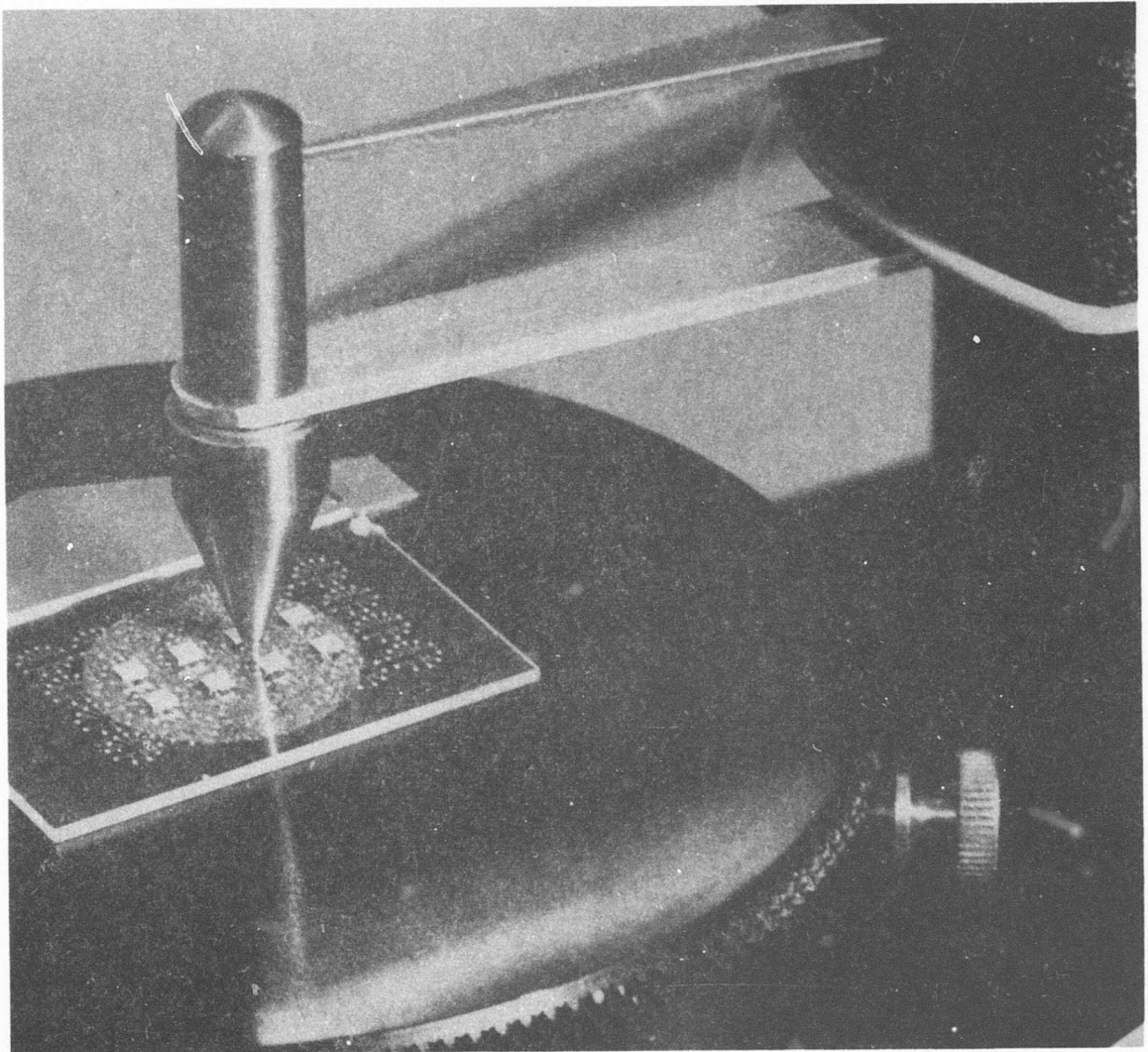
Figure 14. Apparatus Used to Determine Ultimate
Strength of Face-Bonded Bars

Table IX   Face-Bonding Schedule

Cell Numbers[1]	Clamping Force (grams)	Power Duration (seconds)	Power Supply Voltage
1, 3	700	0.6	7.5
2, 4	1200	0.6	7.2
5, 7	1200	0.6	8.0
6, 8	1400	0.6	7.5
9, 11	1100	0.6	8.7
10, 12	1000	0.6	8.5
13, 15	1200	0.6	8.7
14, 16	1300	0.6	8.2

On each planar circuit substrate, bars for temperature compensation were mounted face up using flying leads. This was done to assure that these bars would experience little or no mechanical strain during subsequent thermal cycling. Gold wires, 0.001-inch diameter, were thermocompression bonded to the contact pads on the bar and to the planar circuit with a stress-relief loop between the joints. The bar was held in place only by these flying leads.

The planar circuits with mounted bars were bonded adhesively to 40-pin metal packages. The glass-to-kovar bond area was 0.25 by 0.25 inch and was located as far as possible from face bonds so that the bars would not be affected by any glass-kovar interactions.

After the application of strain gages the pins on the metal package were connected to the planar circuit and to the strain gage contacts. The planar circuit contacts were connected to pins with 0.001-inch diameter aluminum wire. Ultrasonic bonding was employed. The strain gage contacts were connected to pins with 0.002-inch diameter gold wire. Pulse-heated-tip bonding was employed.

Figure 15 shows a specimen ready for use in the program.

3. SPECIMEN INSTRUMENTATION

A primary output variable of this phase was mechanical strain. The primary method of sensing mechanical strain was by means of foil-resistance strain gages.

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1. See Table VIII for Cell Descriptions.
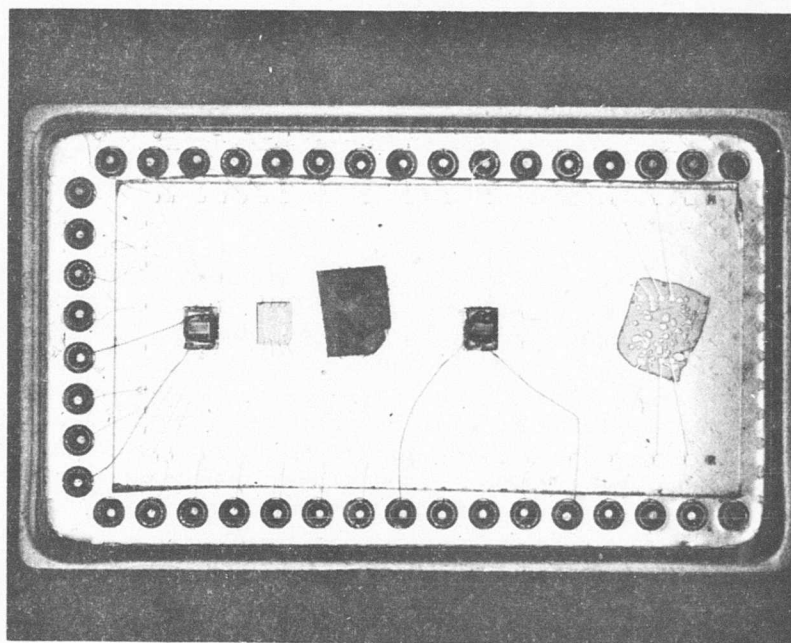
Figure 15. Finished Specimen with Two Face-Bonded Bars (Biaxial Strain Condition) and One Face-Up Bar for Temperature Compensation

The foil gages were to be used to measure strains within their temperature capability and to provide strain calibration of the boron-diffused resistors. The diffused resistors were initially believed to be necessary to measure strains at temperatures above 100C. The boron-diffused resistors were not needed since significant advances were effected in the temperature capability of the foil gages. In order to effect these advances the well-developed foil gage technology was drawn upon extensively and several problems peculiar to this program were solved.

The most evident problem was the small size of the silicon bars. They were 0.100 inch long and 0.080 inch wide. The smallest gage on the market was 0.100 long by 0.020 inches grid width. In order to mount these gages properly it was necessary to trim them by hand to a length of about 0.080 inch. In order to improve this situation, the gage supplier was asked to make a new dimensional configuration. The tab configuration was changed so that the total length was 0.080 inch and the grid width was increased from 0.020 to 0.040. The grid lengths of both types were 0.015 inch. The last half of the gages installed were of this special configuration. The catalog codes for these two types were MA03-015DJ-120 and EA03-015DV-120Q, respectively (supplied by Micromeasurements, Inc.). Thus far gages with longitudinal grids have been discussed.

There was need also for gages with transverse grids for use on half of the specimens from cell numbers 1 through 8, Table VIII. For this purpose a gage otherwise having the same dimensions as the DJ type was used. Its code was MA03-015EH-120.

The small size of the silicon bars precluded the use of full bridge strain gage connections and, considering the numbers of gage installations, it was not convenient to use half-bridge connections. Instead, the specimen measurements were made as quarter bridges and a group of reference gages of each of the three types ennumerated above were also measured as quarter bridges. The readings of the reference gages were averaged by groups and the group averages used as corrections to the readings obtained with the three types of gages.

The reference gages were laid down on silicon wafers (111 out of a single crystal) that were not attached to anything. These devices were subjected to the temperatures used for the thermal cycling of the test specimens so that readings from them showed the effect of temperature on the resistance of the gage alone, and the strain effect created by the thermal incompatibility between the gage metal and the silicon wafer. The thermal coefficient of the gage metal is rated at 3.0×10^{-6} in/in/F, and for the range of -65 to 350 F the thermal coefficient for silicon (111 out) is 1.4×10^{-6} in/in/F. This is an appreciable degree of incompatibility, but unavoidable, because gages of lower thermal coefficient are not normally available.

The gages were bonded to the exposed surfaces of silicon bars with BR 600 adhesive (supplied by Micro Measurements, Inc.). This is a specially prepared epoxy resin intended for the bonding of strain gages. It has a higher working temperature range than resins available for this use at the time the proposal for this program was written. In other words, the older high-temperature resins required a high curing temperature, which, it was feared, would cause premature failures in the test specimens. The BR 600 may be cured at 107 C (1 hour) and is recommended for service to 210 C. This advanced bonding agent obviated the need for the boron-diffused resistors.

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The actual operation of bonding the gages down to the silicon devices uncovered two problems. First it was found that there was danger that resin would flow under the silicon bar. This was prevented by using small compact pads of absorbant tissue during curing to absorb the excess at the flow stage. The other problem was a matter of obtaining good adhesion to the silicon surface. Early in the bonding operation most of the gages laid down peeled off when the clamps were removed. The silicon surface had been sponged with acetone and then neutralizer in accordance with standard procedures. The use of other conventional cleaning solvents and abraiding of the silicon dioxide surface with abrasive cloth did not offer improvement. Dimethyl sulfoxide was then used as a cleaning solvent and the difficulty was overcome. (In the course of this effort, it was noted that one batch of cotton swabs supplied to us appeared to have been treated with some agent intended to keep the cotton floss tightly attached to the end of the stick. This may have been a silicone and a strong contributor to our inability to make good strain-gage bonds.)

The glass substrate to which the silicon bars were face bonded was bonded into the 40-pin package or carrier with a polyester film adhesive. The strain gages were wired to the assigned pins on the package with gold wires attached to the strain gage tabs by means of a modified form of thermocompression bonding. The leads from the package to the strain indicator were soldered to the package pins with high-temperature soft solder.

The three-wire system of leads was used to provide lead resistance compensation, a very desirable feature for these tests because about half the length of the copper leads was heated or cooled within the oven during the temperature cycling tests. Otherwise the change of resistance of the lead wires would appear as error in the results.

4. DATA ACQUISITION

This part of the report deals with tests performed after the assembly of the devices had been completed as shown in Figure 15. The types of tests may be enumerated as thermal-strain tests, circuit electrical continuity, metallographic examination of the face-bonded joints, and a determination of the thermal coefficient of expansion of the two glasses employed as substrates.

There were three purposes for performance of the strain tests: first, to determine the magnitudes of the strains in the silicon bars in order to compare to compare the effects of the various design and bond parameters; second, to obtain indications of failures on the attachments of the silicon bars to the substrate; and third, to obtain precise values of thermal expansion of the two types of glass substrates.

Some information has already been given about the method of the installation of the gages on the silicon bars. (The gages were installed on samples of glass in a similar manner.) The gage readings were indicated on a Model 205 Digital Strain Indicator manufactured by Binary Electronics Corp. This equipment is based upon the usual Wheatstone Bridge and is automatically balanced by a servomotor. It has a binary coded decimal output. This output is recorded by a Model 561B Hewlett-Packard printer. The strain indicator reaches a balance in 0.5 to 1.0 second and the printer requires an additional 200 milliseconds to print a reading. The strain gages are wired to the strain indicator by means of balance and control units. These units

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provide a zero-balancing rheostat for each circuit and are equipped with circuit switching coordinated with the H-P printer, so that when a gage has been balanced and its value printed on a tape in the printer, the next gage in order is switched to the indicator. This feature of advancing to the next gage continues automatically until all the gages under test have been balanced and their readings recorded. It is thus possible to record the readings of a group of gages in less than one second, on the average, per gage.

With this capability possible, it was made a matter of practice to take a number of repeated readings for each point. In working up the data, the first step is to average these multiple readings. Then the averaged readings of the several reference gages are subtracted from the values obtained from the active gages of corresponding type. The resulting values may then be plotted for graphical presentation.

Circuit electrical continuity was measured using a Triplett Voltohmmeter, Model 630A. The nominal circuit resistance was approximately 85 ohms. A resistance in excess of 90 ohms was considered to indicate a damaged or degraded circuit.

Metallographic preparation of selected samples was accomplished by encapsulating the sample (as shown in Figure 15) in an epoxy resin, removing the bottom of the 40-pin can by wet grinding on silicon carbide sanding paper, and encapsulating again to position the specimen for selective cross sectioning of face bonds. Special care was taken during the initial grinding to avoid disturbing the glass substrate. During the cross sectioning of the face bonds, special care was taken to avoid chipping and spalling of the glass and the silicon.

The infrared microscope (thermal scan) has been used to evaluate diffusion bonds on integrated circuits.(2) A similar attempt was made in this program to evaluate face bonds. Using a Barnes Engineering Model RM-2B infrared microscope with a 15x optical objective (0.0028 inch spot size) a face-bonded silicon bar was scanned. The silicon bar was at a temperature of 45 C over most of its area. At face bonds, the temperature increased to 48 to 49 C. This temperature rise showed a capability to detect the presence or absence of a bond column. Determination of defective bonds (where the bond column was present) was not so straightforward. Although the equipment has such potential, it became obvious that calibration for this purpose would entail such a large effort and such a long flow time as to be outside the scope of this program. Therefore, this potential inspection technique was not employed.

The inspection technique which was used was visual examination at magnifications ranging from 10 to 100 power. By looking through the glass substrate (after dissolving the adhesive and removing it from the package), a semi-quantitative estimate of bond quality could be made after the bonds were known to exhibit electrical continuity. Such features as glass breakage under bonding sites and damage to the metallization were readily detectable.

5. DATA REDUCTION

The strain-gage indications were manipulated and tested for validity in the following manner. Six readings were taken at each datum point and the average of these, excluding obvious outliers, was accepted as the output value for the datum point. This produced six values per gage for each temperature cycle. Each cycle started at 24 C with zero strain being indicated. In order for the data from a cycle

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to be accepted, the cyclic return to zero strain at 24 C had to be less than 100 micro-inches per inch. Cyclic data not conforming to this requirement were rejected as invalid. The general import of this procedure was to cause rejection of data from cycle numbers one and two. In a few instances the data from cycle number three was also rejected for cause.

Another test of validity was that gages which indicated decreasing strain with increasing temperature were considered to be bonded unacceptably to the silicon bars. Data of this characteristic were rejected unless all points were within the range of ± 100 microinches per inch after considering zero shifts.

Table X presents the results of testing the data for validity in the foregoing manner.

Table X. Data Yield from Strain Gages

Cell Number[2]	Number of Strain Gages		
	Total	Invalid	Valid
1	8	3	5
2	8	5	3
3	8	3	5
4	8	3	5
5	8	3	5
6	8	0	8
7	8	1	7
8	8	1	7
9	9	9	0
10	9	5	4
11	9	5	4
12	9	7	2
13	9	7	2
14	9	2	7
15	9	7	2
16	9	5	4

2. See Table VIII for cell descriptions.

The results from valid strain gages were examined for detectable or nondetectable force link (the term, "force link," is used herein to denote the transmission path of forces between the glass substrate and the silicon bar) with the glass substrate. The data from each valid gage was judged for attribute according to the criteria shown in Figure 16. When all of the data from a strain gage was contained in the horizontal nondetect zone, it was judged that no significant force link was operative. Conversely, when the data fell within the detect zone, it was judged that an effective force link operated. Zero shifts were considered, especially in marginal cases.

Note also the theoretical maximum line bounding the detect zone in Figure 16 This is the maximum strain which a silicon bar could experience assuming the glass substrate to be infinitely rigid and assuming infinitely rigid and infinitely strong face bonds. (This line is the difference between the expansion of the glass substrate and the expansion of the silicon bar.) This assumption is not rigorously true, but, for practical considerations, it is very nearly true because of the fact that the glass is five times as thick as the silicon bars.

The results of electrical continuity testing were reduced by statistical methods. The basic assumptions were:

1. The experimental units within a set are assumed to be homogeneous.

2. The number of failures within each set is taken to follow the binomial probability law.

One set was lost due to failures in construction. The treatment combination corresponding to the lost set was Cell No. 9, Table VIII.

With the above assumptions each set of experimental units is treated as coming from a separate binomial population. It was then possible to get at least six and in some cases seven independent tests of the effect of each factor. For example, the substrate is represented in all the sets; i.e., seven have the soft glass and seven have the 7059 glass. Neglecting the possible interactions, a typical test would be to look at the difference between:

Set 1: 7059, uniaxial, aluminum, 0.001 inch

Set 2: Soft, uniaxial, aluminum, 0.001 inch

The hypothesis to be tested is H_0: $p_1 = p_2$ against the alternative H_A: $p_1 < p_2$. Where p_1 corresponds to the proportion of failures in Set 1 and p_2 corresponds to the proportion of failures in Set 2.

If the hypothesis is not rejected at a probability of 0.05 or lower, it is assumed that there is no difference in the two treatment combinations. That is, there is no difference between soft and hard glass in the substrate. If the hypothesis is rejected, then it is taken to mean that 7059 glass has significantly fewer failures than soft glass in this particular set of treatment combinations.

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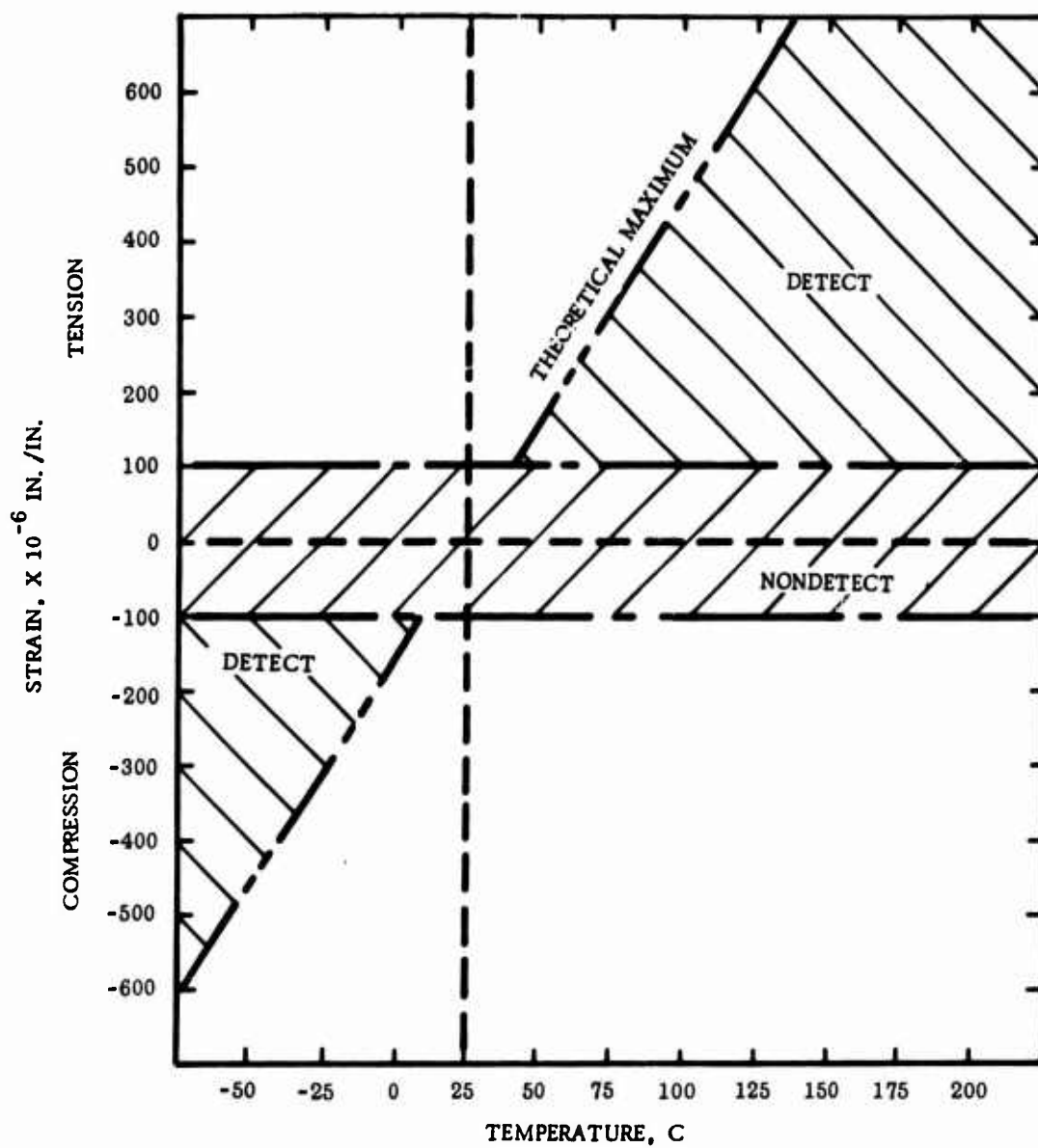
Figure 16. Thermal Strain in Face-Bonded Silicon Bars, Force-Link Criteria

The statistical test used in testing the above hypothesis is the standard test on two binomial proportions given by Stuart & Kendall and is commonly referred to as the exact test. (3) Following the procedure explained above, six or seven independent tests of the hypothesis are formed and the significance levels of these tests are combined by a method given by R. A. Fisher for combining independent tests of significance. Fisher's method is explained fully in an article by Allan Birnbaum. (4)

RESULTS

1. THERMAL STRAIN

The reduced thermal strain data are presented in Table XI. Figure 17, (a) through (e), presents data typical of that which were reduced to produce Table XI. Figure 18 presents the experimentally determined thermal expansion behavior of the glass substrates and of the silicon bars. The data in Figure 18 were used to construct the theoretical maximum lines in Figure 17.

The information in Table XI has been further reduced and is presented in Table XII in a manner which indicates the effects of assembly design parameters on thermal strain.

Table XI. Summary of Thermal Strain in
Face-Bonded Silicon Bars

Cell Number[3]	Force Link Between Silicon Bar and Glass Substrate	
	Detect	Nondetect
1^4	3	2
2	3	0
3^4	4	1
4	3	2
5	1	4
6	6	2
7^4	6	1
8	2	5
9	0	0
10^4	2	2
11	0	4
12	0	2
13	1	1
14	3	4
15	0	2
16^4	1	3

2. ELECTRICAL CONTINUITY

Figure 19 presents the results of electrical continuity testing after three temperature cycles. All circuits exhibited continuity in the as-fabricated condition.

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3. See Table VIII for cell description.

4. Typical data detailed in Figure 17.

SILICON BAR NO	-	33-5	36-5	33-7
STRAIN DIRECTION	-	T**	T	L**
SYMBOL*	-	O	△	■

SILICON BAR NO.	-	36-7	34-5
STRAIN DIRECTION	-	L	T
SYMBOL*	-	●	▲

**L = LONGITUDINAL
T = TRANSVERSE

*SOLID SYMBOLS INDICATE BARS
EXHIBITING OPEN ELECTRICAL CIRCUITS
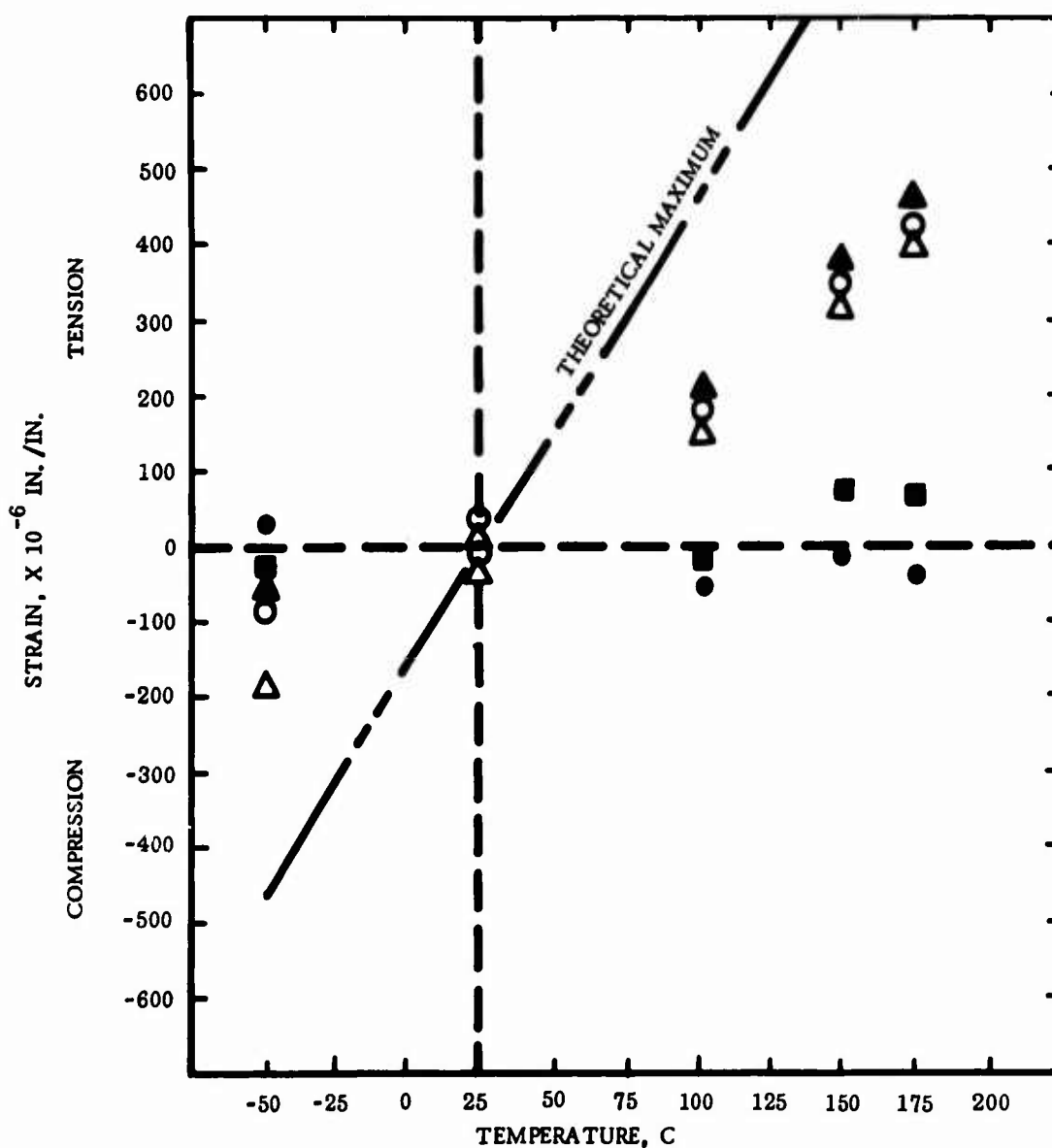
(a) Experimental Cell No. 1 (See Table VIII)

Figure 17. Thermal Strain in
Face-Bonded Silicon Bars

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SILICON BAR NO.	-	40-5	40-7	38-7
STRAIN DIRECTION	-	L	T	T
SYMBOL*	-	O	△	□

SILICON BAR NO.	-	39-5	38-5
STRAIN DIRECTION	-	T	L
SYMBOL*	-	◇	●

*SOLID SYMBOLS INDICATE BARS EXHIBITING
OPEN ELECTRICAL CIRCUITS
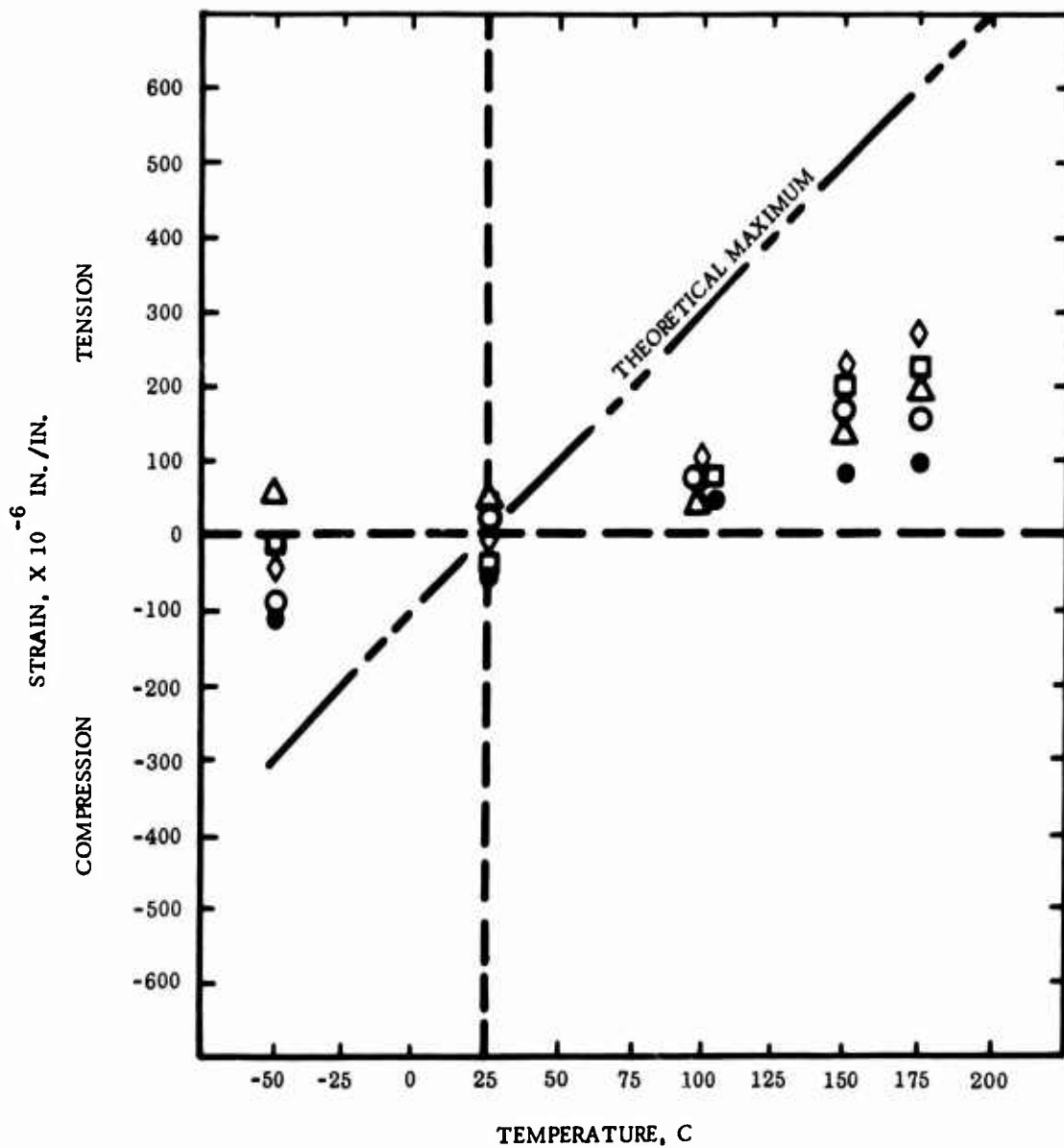
(b) Experimental Cell No. 3. (See Table VIII)

Figure 17. (Continued)

41

SILICON BAR NO.	-	19-3	19-4
STRAIN DIRECTION	-	T	L
SYMBOL*	-	O	△

SILICON BAR NO.	-	21-1	21-4
STRAIN DIRECTION	-	L	L
SYMBOL*		□	●

*SOLID SYMBOLS INDICATE BARS EXHIBITING
 OPEN ELECTRICAL CIRCUITS
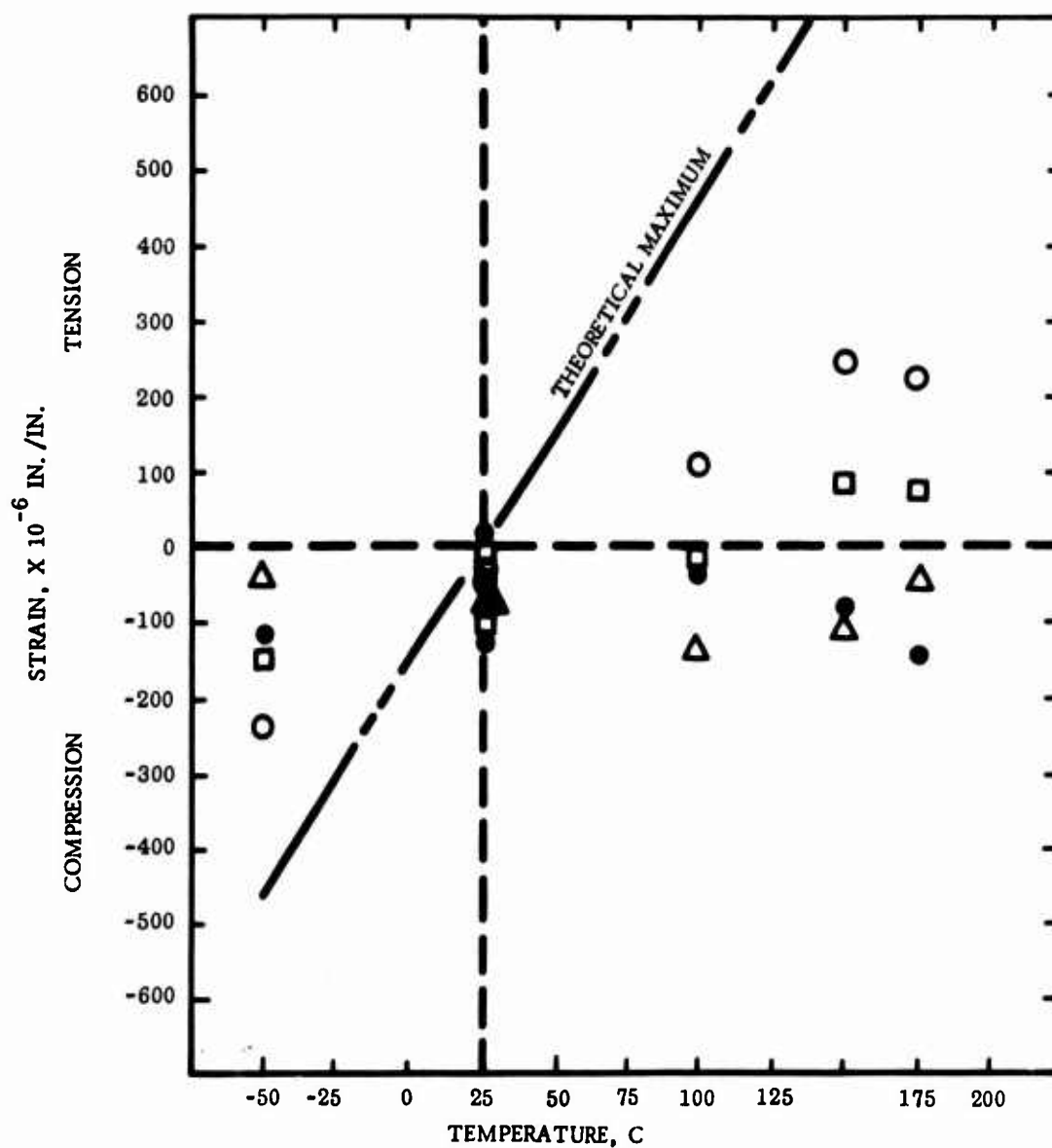
(c) Experimental Cell No. 10. (See Table VIII)

Figure 17. (Continued)

SILICON BAR NO.	-	53-5	56-5	56-7	
STRAIN DIRECTION	-	L	L	L	
SYMBOL*	-	O	△	□	
SILICON BAR NO.	-	54-5	53-7	55-5	55-7
STRAIN DIRECTION	-	T	T	L	L
SYMBOL*	-	◊	⬡	D	⬠

*SOLID SYMBOLS INDICATE BARS EXHIBITING
OPEN ELECTRICAL CIRCUITS
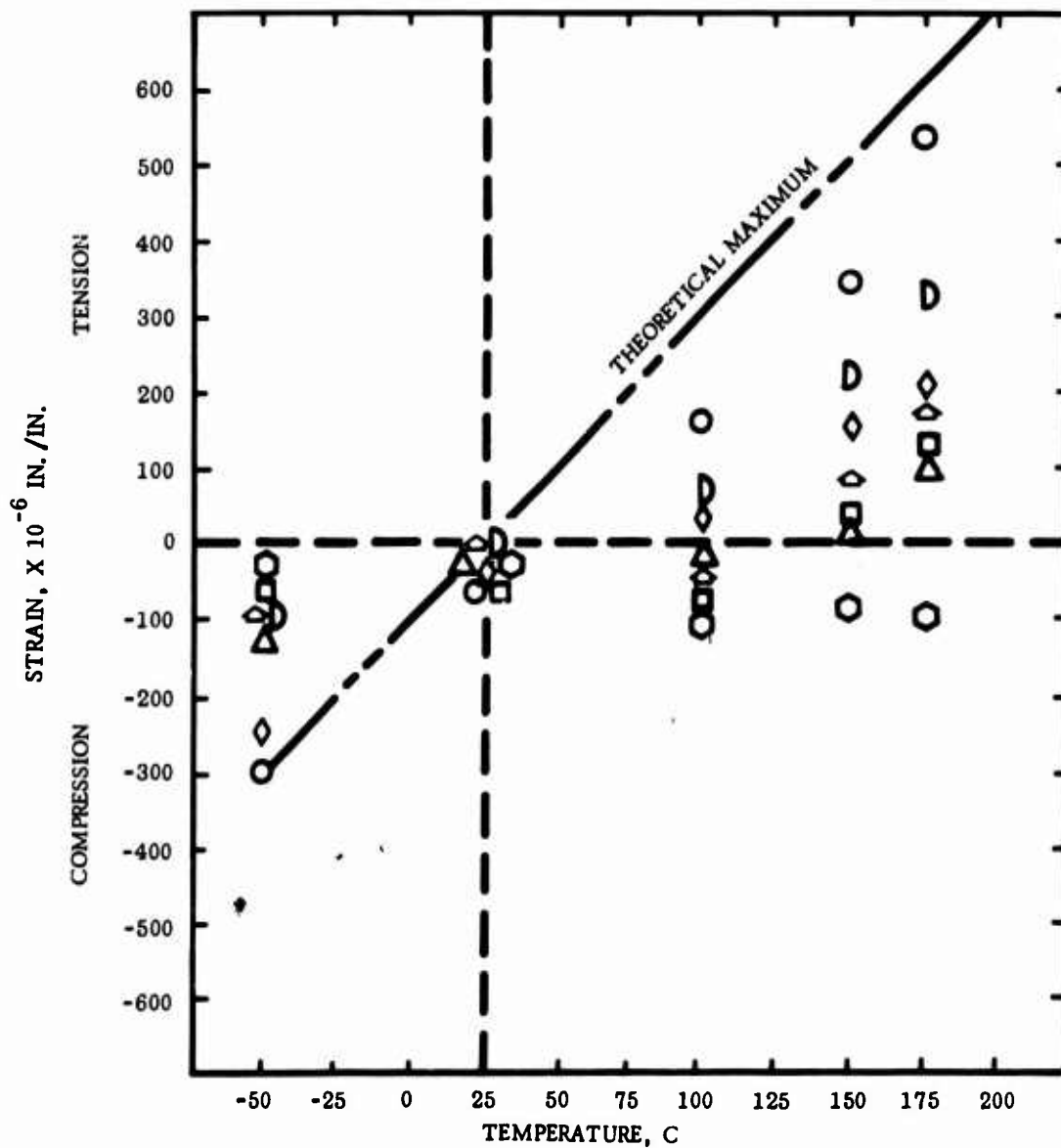
(d) Experimental Cell No. 7. (See Table VIII)

Figure 17. (Continued)

43

SILICON BAR NO.	-	18-1	18-3
STRAIN DIRECTION	-	L	L
SYMBOL*	-	◯	△

SILICON BAR NO.	-	17-4	17-3
STRAIN DIRECTION	-	L	L
SYMBOL*	-	▢	◇

*SOLID SYMBOLS INDICATE BARS EXHIBITING
OPEN ELECTRICAL CIRCUITS
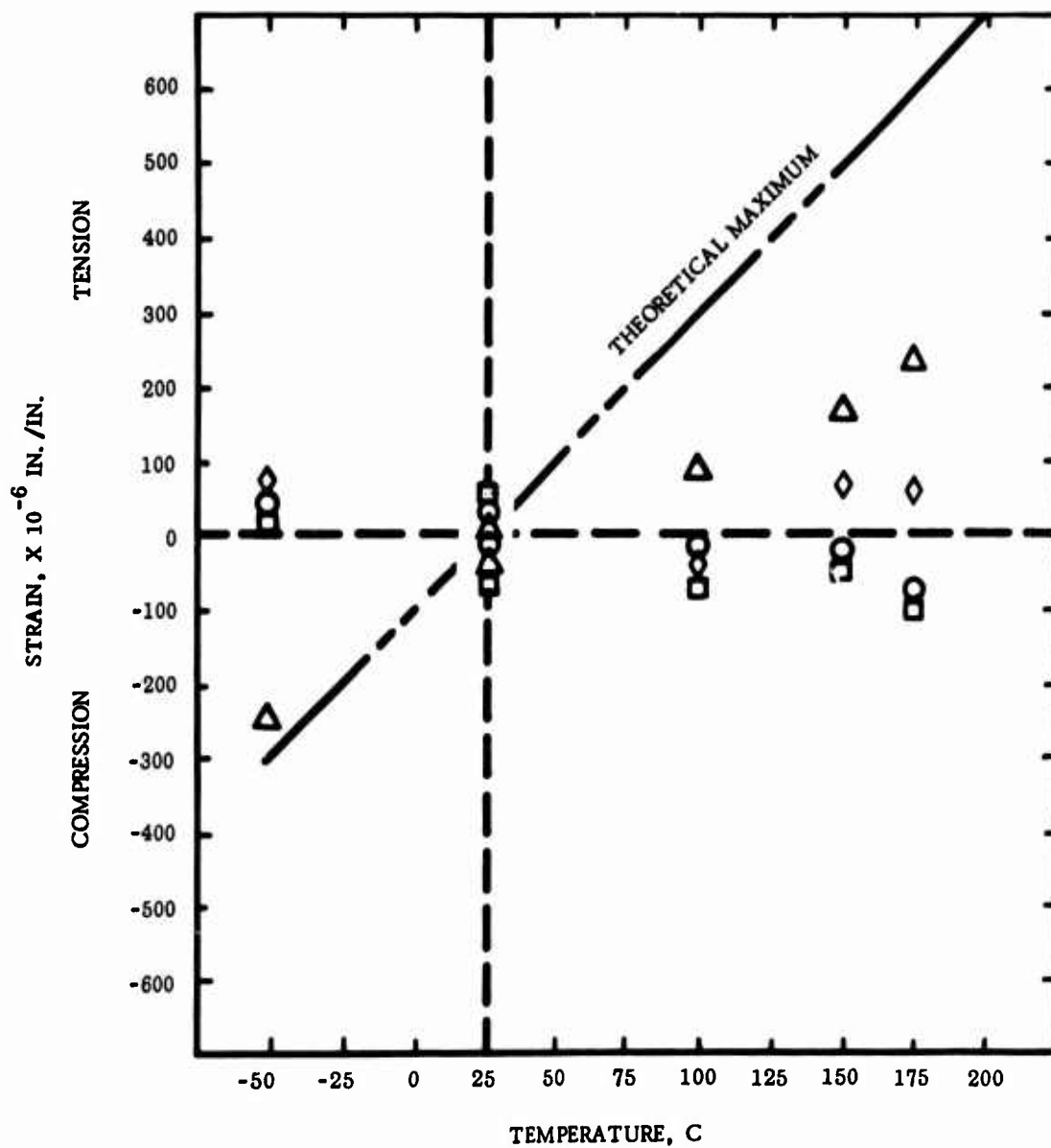
(e) Experimental Cell No. 16. (See Table VIII)

Figure 17. (Concluded)

44
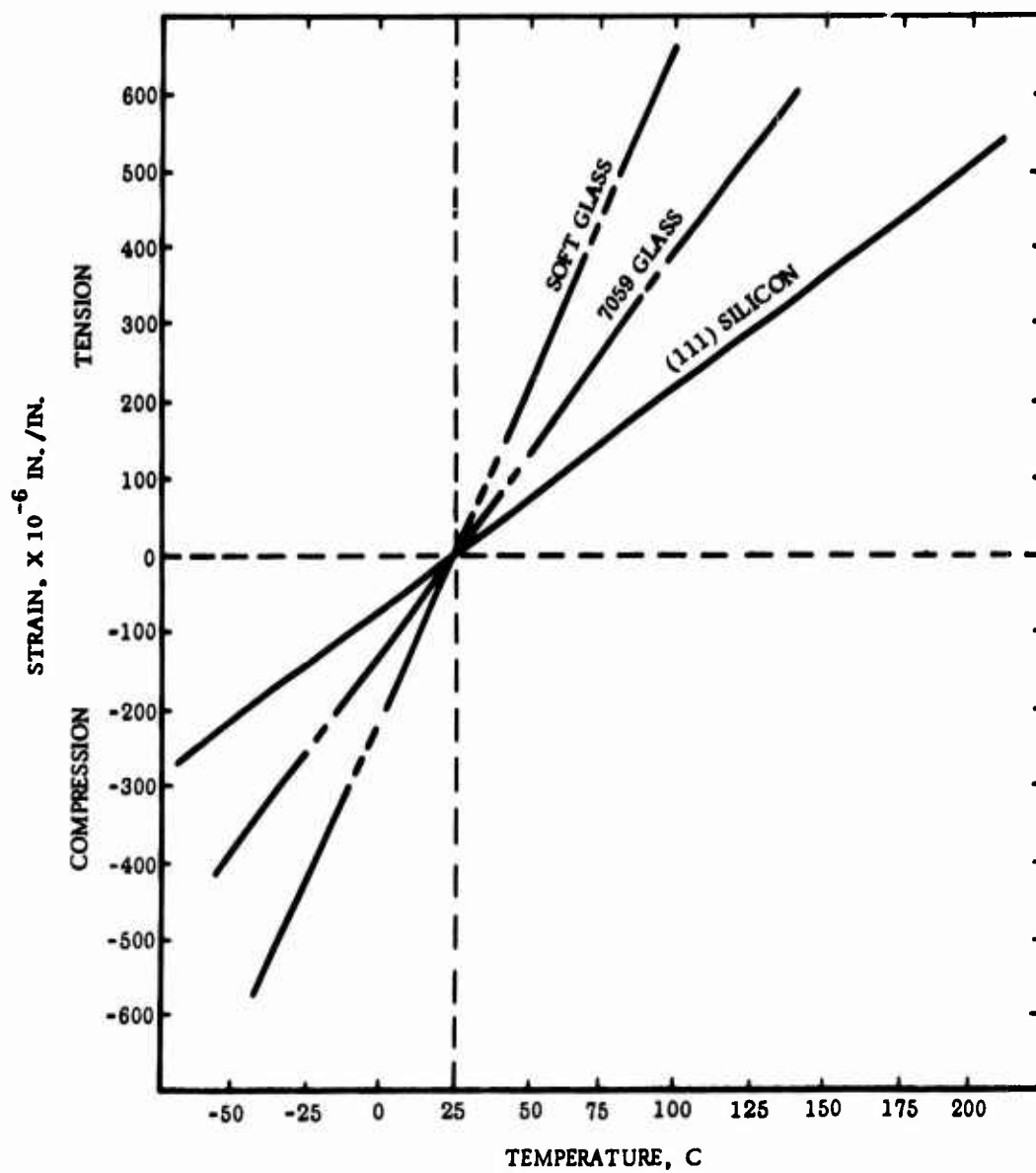
Figure 18. Thermal Expansion of Glass
Substrates and Silicon Bars

45
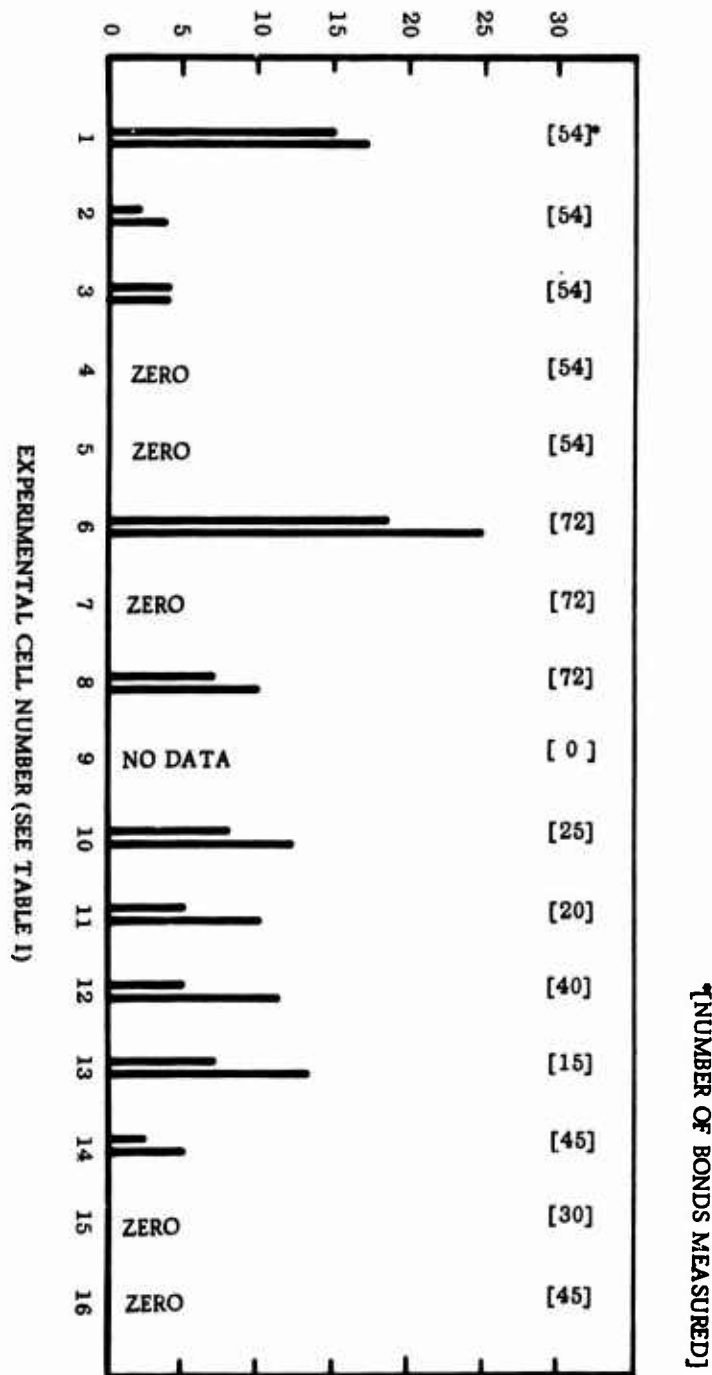
Figure 19. Results of Post-Thermal-Cycling
Electrical Continuity Testing

46

Table XII. Effect of Assembly Design Parameters on
Force Link in Face-Bonded Assemblies

Assembly Design Parameter[5]	Design Parameter Value[5]	Force Link: Percent Nondetect[6]
Strain Condition	Uniaxial	72
	Biaxial	38
Substrate Material	Soft Glass	44
	7059 Glass	56
Bond Material	Gold	46
	Aluminum	52
Bond Height (fabricated)	$2 - 3 \times 10^{-4}$ inches	50
	$8 - 10 \times 10^{-4}$ inches	50

Note that two levels of failure rate are indicated for each experimental cell in Figure 19. The reason for this was that each circuit encompassed two face bonds. If a circuit was found electrically open, one or both bonds could have been damaged. In some cases each of the two could be isolated and checked. In other cases isolation was not possible. Thus the two indicated levels are the possible extreme limits.

The data in Figure 19 were reduced as discussed in II.5 to indicate the effects of assembly design parameters on post-thermal-strain electrical integrity. The results of this reduction are:

Test 1: H_O: $P_1 = P_2$

H_A: $P_1 < P_2$

1. Corresponds to 7059 glass substrate.

2. Corresponds to soft glass substrate.

---

5. See Table VIII

6. Based on data from Table XI.

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It was possible to form six independent tests of this hypothesis and the combination of these results led to the rejection of H_0. The conclusion then is that 7059 glass gives significantly fewer failures than soft glass.

Test 2: H_0: $P_1 = P_2$

H_A: $P_1 < P_2$

1. Corresponds to uniaxial strain condition.

2. Corresponds to biaxial strain condition.

It was possible to form six independent tests of this hypothesis and the combination of these results led to the rejection of H_0. The conclusion then is that uniaxial strain condition gives significantly fewer failures than biaxial strain condition.

Test 3: H_0: $P_1 = P_2$

H_A: $P_1 < P_2$

1. Corresponds to aluminum bonding material.

2. Corresponds to gold bonding material.

There were seven tests here that could be combined and the results from the seven independent tests led to the rejection of H_0. Therefore, it is concluded that aluminum bonding material results in significantly fewer failures.

Test 4: H_0: $P_1 = P_2$

H_A: $P_1 < P_2$

1. Corresponds to 2 to 3×10^{-4} inch bond height.

2. Corresponds to 8 to 10×10^{-4} inch bond height.

This test led to the combination of six independent tests and the result was significant. H_0 was rejected, and it is concluded that the height of $2 - 3 \times 10^{-4}$ inch gives significantly fewer failures than the $8 - 10 \times 10^{-4}$ inch height.

These reduced results are summarized in Table XIII.

3. METALLOGRAPHIC ANALYSIS

Typical photographs of metallographic sections are presented in Figure 20, (a) through (f). Figure 20, (a) through (d), shows face bonds which exhibited electrical continuity after the temperature cycling. Figure 20, (e) and (f), shows face bonds from circuits which were electrically open after the temperature cycling. Note that

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Table XIII. Effect of Assembly Design Parameters on Post-
Thermal-Cycling Electrical Continuity

Assembly Design Parameter[7]	Design Parameter Value[7]	Lowest Number of Electrical Failures[8]
Strain Condition	Uniaxial	X
	Biaxial	
Substrate Material	Soft Glass	
	7059 Glass	X
Bond Material	Gold	
	Aluminum	X
Bond Height (fabricated)	$2 - 3 \times 10^{-4}$ in.	X
	$8 - 10 \times 10^{-4}$ in.	

in each case one of the two examples shows probable electrical continuity. Of particular significance in Figure 20, (e) and (f) is the lazy-S shape of the bonds which are marking electrical contact.

A number of other circuits which exhibited electrical discontinuity after temperature cycling were also analyzed. Silicon bar number 42-7, Cell No. 2, was found to have a fracture in the silicon which caused the electrical open. The fracture was probably due to handling. Silicon bar No. 31-5, Cell No. 8, was fractured in the same manner as silicon bar No. 42-7. Silicon bar number 22-1, Cell No. 12, was found to have damaged metallization on the bar which appeared to have been caused by an electrical overload. Silicon bar No. 27-7, Cell No. 6, was out of parallel with the glass substrate, a result of handling damage.

4. VISUAL EXAMINATION

A number of silicon bars were examined for bond-site damage after temperature cycling by observing through the glass substrate as depicted in Figure 21. This examination was performed primarily to detect differences related to bond material and was capable of detecting damaged metallization and damaged glass (see Figure 22). Table XIV presents the results of this examination.

7. See Table VIII.

8. Based on data in Figure 19 and marked as "X."

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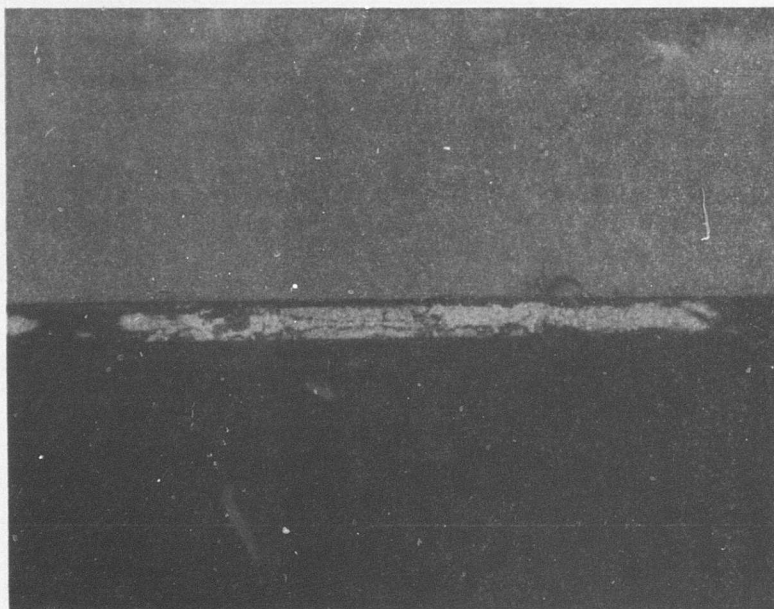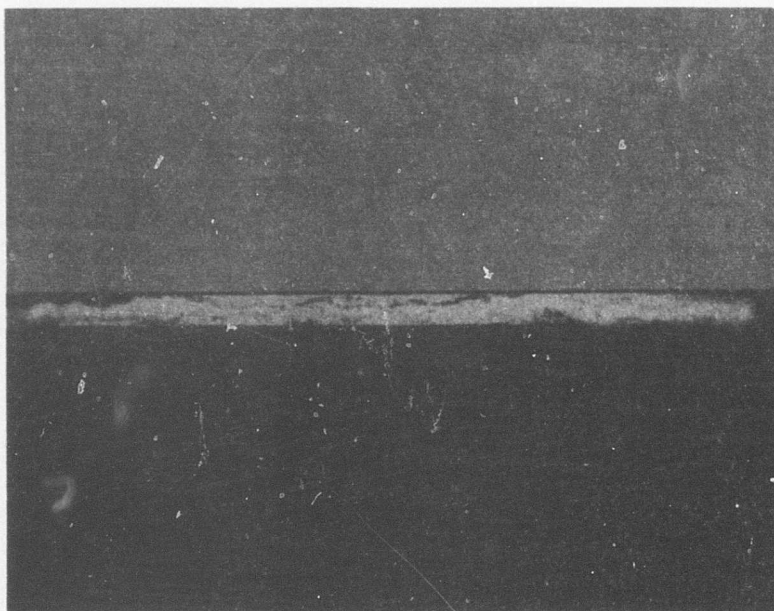
(a) Experimental Cell No. 3 Electrically Closed, Silicon Bar No. 37-7 (See Table VIII)

Figure 20. Metallographic Characteristics of Face Bonds, 630X
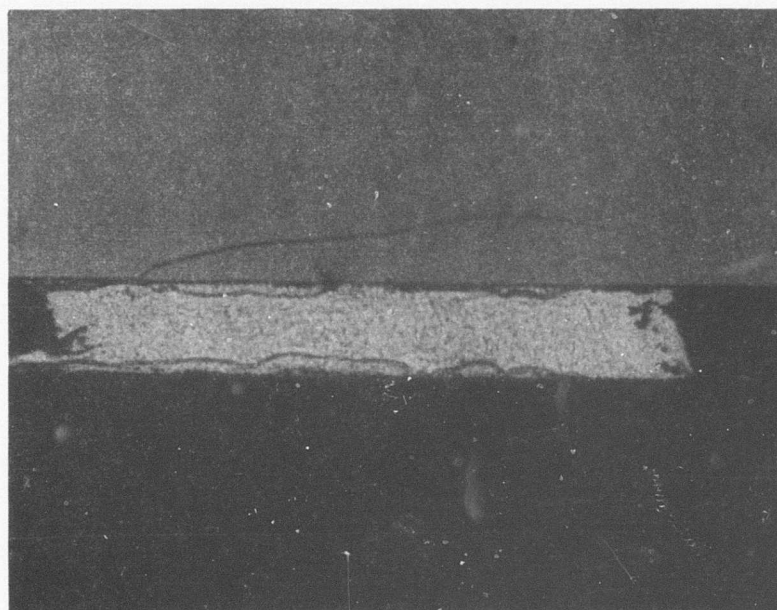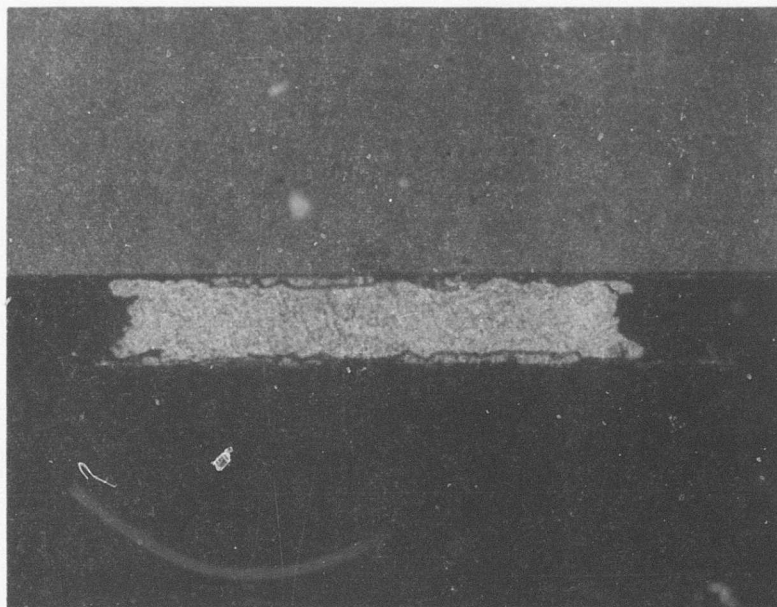
(b) Experimental Cell No. 4 Electrically Closed, Silicon Bar No. 46-7 (See Table VIII)

Figure 20. (Continued)
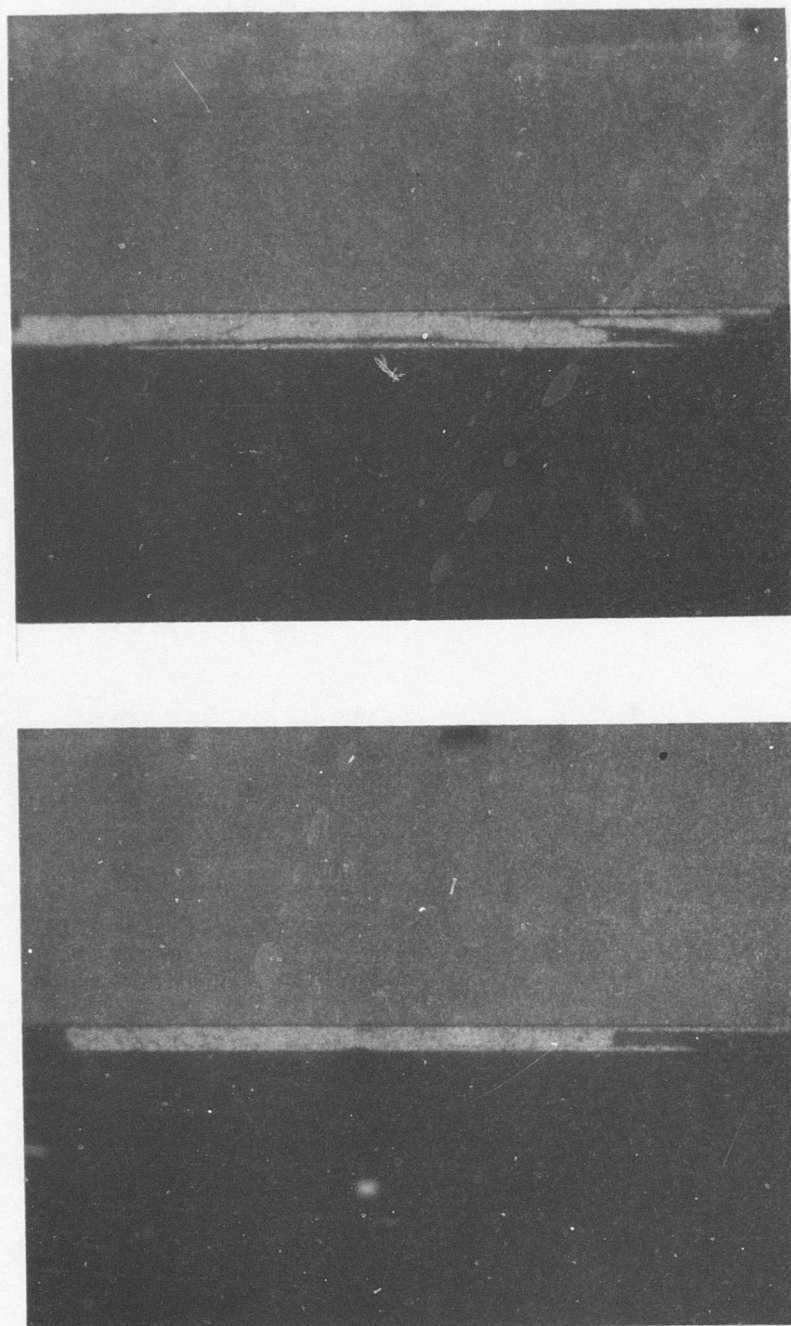
(c) Experimental Cell No. 5 Electrically Closed, Silicon Bar No. 49-7 (See Table VIII)

Figure 20. (Continued)

52
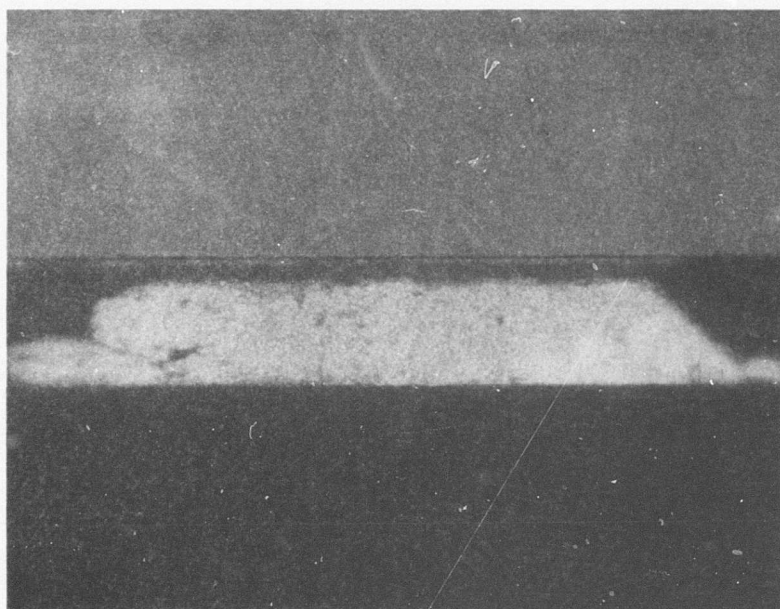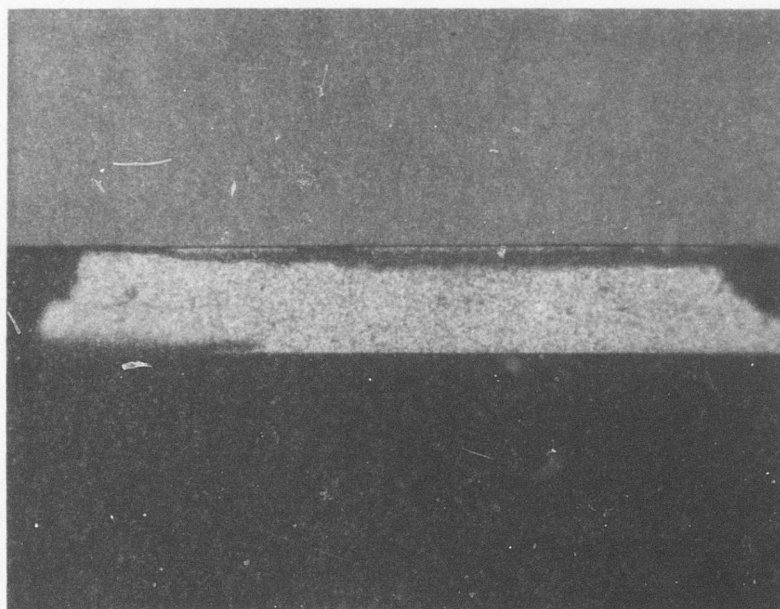
(d) Experimental Cell No. 6 Electrically Closed (Confirmed by Sequential Sectioning), Silicon Bar No. 28-7 (See Table VIII)

Figure 20. (Continued)

53
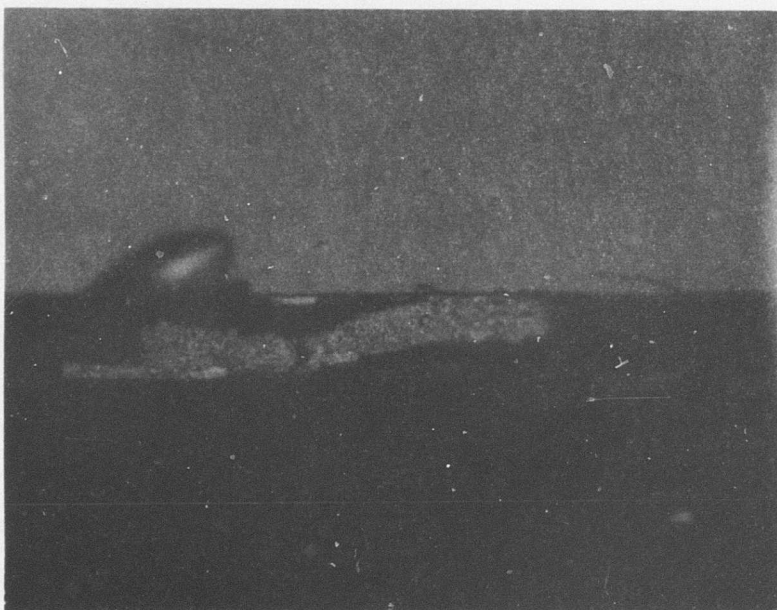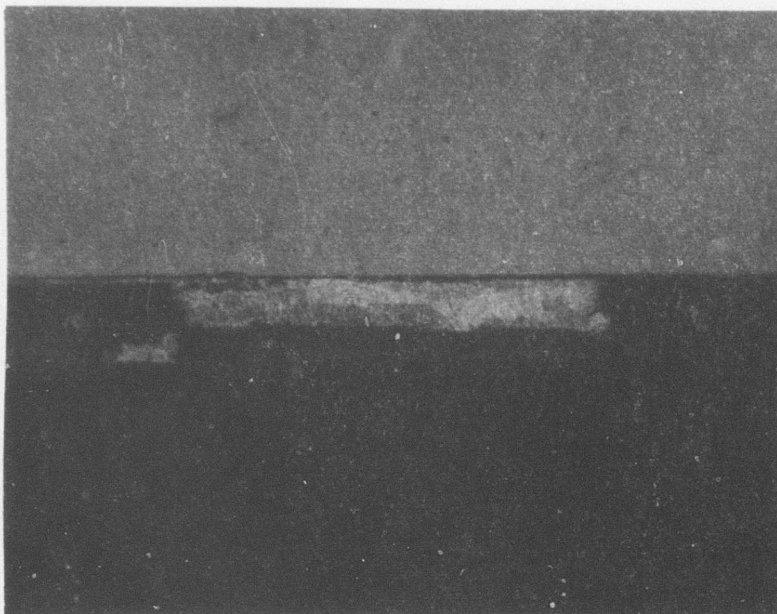
(e) Experimental Cell No. 1 Electrically Open, Silicon Bar No. 34-5 (See Table VIII

Figure 20. (Continued)

54
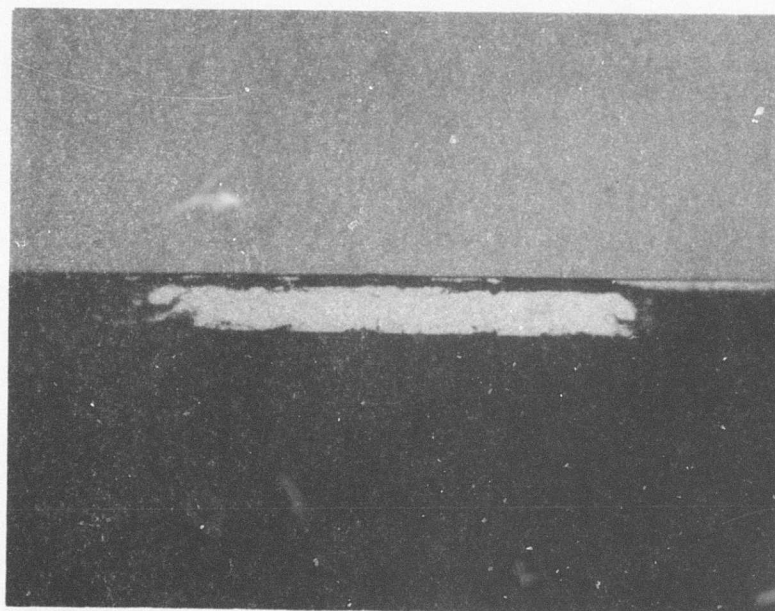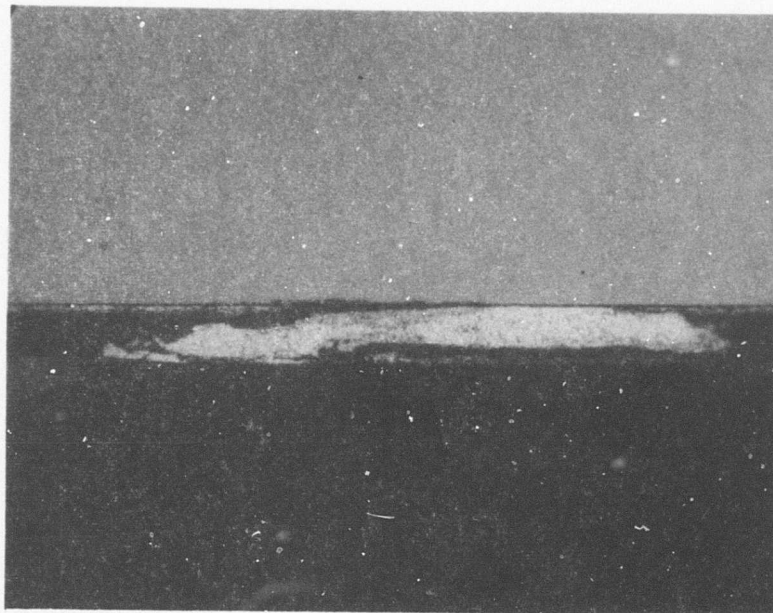
(f) Experimental Cell No. 3, Silicon Bar No. 38-5 (See Table VIII)

Figure 20. (Concluded)

55
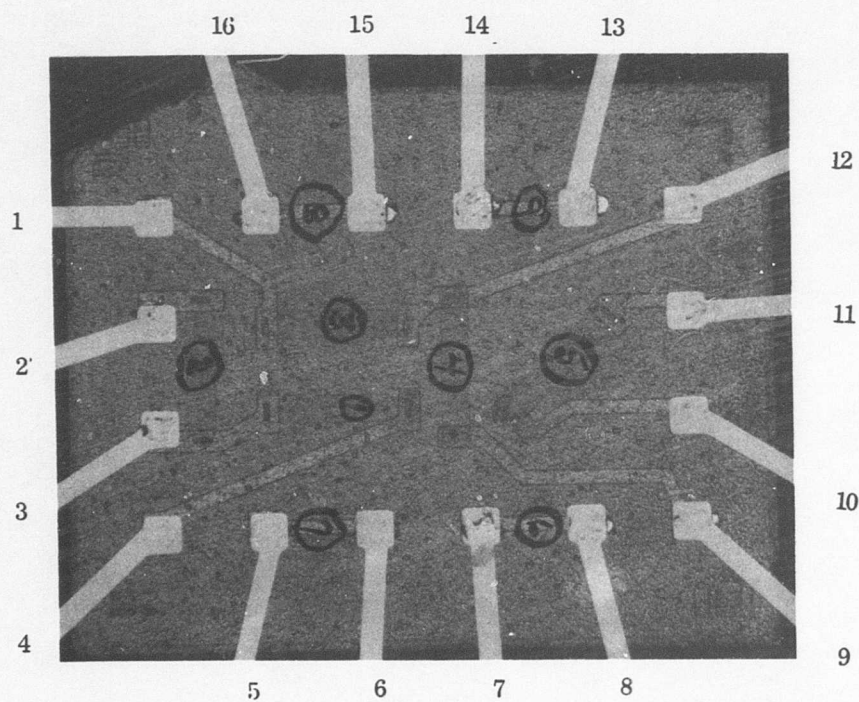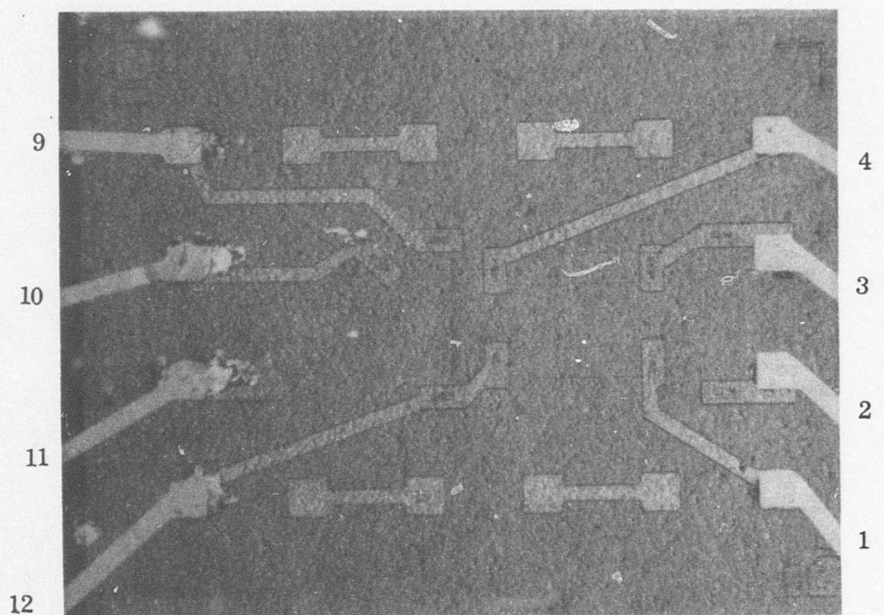
Figure 21. Visual Examinations for Bond-Site Damage
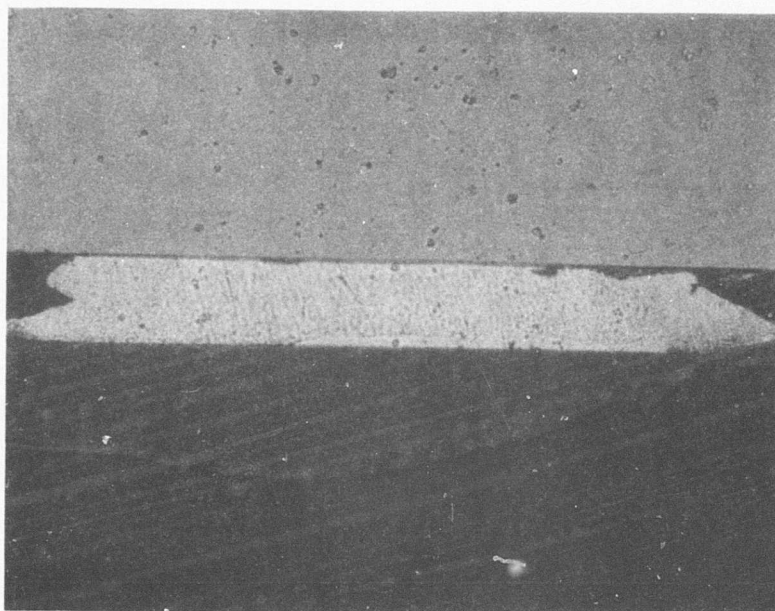
Figure 22. Damaged Glass at Bond Site

Table XIV. Bond-Site Damage

Bond Material	Number of Sites Examined	Percent of Sites Damaged
Gold	200	35
Aluminum	176	6.3

DISCUSSION

The primary objective of Phase II of the program is to define the effects of assembly design parameters such that a "practical best" design for use in Phase III can be established.

No single one of the output variables can provide the sole basis for accomplishing the objective. First, no single output variable can provide information on all points of concern. Second, no single output variable was measured with great precision.

The measurements of thermal strain did provide quantitative estimates of the strain levels which each design might exhibit. (The corresponding stress levels may be calculated by multiplying the strains by 27×10^6 psi.) However, these measurements shed no light on failure mechanism and, at this time, very little light on failure rate. Further, the force-link attribute was defined arbitrarily as to efficiency and imprecisely as to magnitude.

The electrical measurements, although quite precise in themselves, could not distinguish between significant failures and trivial failures. One assumes that trivial failures were scattered randomly throughout the experimental matrix. The electrical measurements revealed nothing with respect to failure mechanism of strain in the assembly.

The metallographic analyses revealed the limitations on the other output variables and the failure mechanism. These results did not provide estimates of either strain or failure rate. They did, however, shed light on the long-term reliability projection and on some specimen fabrication effects.

The visual examination of bond sites was qualitative, and as such was not necessarily performance related. Further, this examination had very little capability to discriminate between real bond-site damage and discoloration due to the formation of gold-aluminum compounds. This examination had no capability to measure either strain, electrical failure, or failure mechanism. The examination did, however, detect with good precision the bond sites which were not damaged.

Thus, all of the output variables must be used in concert and in context to establish the "practical best" design for Phase III. The selection of the "practical best" design is based on four criteria. First, the packing density sought with face bonding should not be compromised. Second, the silicon bar should not be strained unduly during temperature changes. Third, the face bonds should be resistant to electrical degradation during temperature changes. Fourth, the face bonds should be stable metallurgically to ensure long-term reliability.

With these criteria in mind, the results can be analyzed to select the best level of each assembly design parameter.

Selection of the bond height seems relatively straightforward. The data in Table XII indicates that bond height is not particularly effective in changing the strain. in the silicon bar. The metallographic information indicates no change in failure mechanism with bond height. The data in Table XIII indicate that the 2 to 3 x 10^{-4} inch bond height is the preferred level from the electrical continuity standpoint. Thus, it is judged that the 2 to 3 x 10^{-4} inch bond height is best.

Selection of substrate material is similarly clearcut. The data in both Tables XII and XIII indicate selection of the 7059 glass. The other output variables do not discriminate. Thus, it is judged that the 7059 glass is best.

Selection of bond material can be based upon electrical continuity testing, metallographic analyses, and bond-site examination since the data in Table XII does not discriminate. The data in Table XII indicate that the lowest electrical failure rate was experienced with aluminum bonds. The data in Table XIV indicate much less bond-site damage for aluminum than for gold. The metallographic information shows clearly that the gold bonds are composed of gold plus a significant amount of gold-aluminum intermetallic compounds which are known to increase in amount with time and temperature. (5) These compounds apparently activate a brittle fracture mechanism which was not observed in aluminum bonds. Further, extensive damage to the glass under the bond pads was often observed with gold bonds, but seldom with aluminum bonds. Finally, the aluminum bonds were observed to assume the same compliant shape, the lazy-S, as is illustrated for the gold bonds in Figure 20, (e) and (f), but without the brittle fracture tendency. The lazy-S configuration provides the essence of an eccentrically loaded Euler column which buckles noncatastrophically during the temperature cycling. Note in Figure 20 that the plane of observation is transverse to the lazy-S. This provides substantial strain relief to the silicon bar. So long as the ends of this Euler column remain fastened to the bond pads, the partial fracture between bond and pad, necessary to form the lazy-S, is a desirable feature. Further, the intrinsic properties of aluminum are such that at the higher temperatures, where tensile strain on the silicon bar is greatest, the aluminum will flow plastically with minimal work hardening and embrittlement. Thus, it is judged that aluminum is the best bonding material.

The most advantageous bonding pattern (nominal strain state) is, from the results, uniaxial. Table XII indicates an overall strain relief advantage. This may be seen graphically in Figure 17 by comparing Cell No. 1 to Cell No. 10 and Cell No. 7 to Cell No. 16. Table XIII indicates fewer electrical failures for the uniaxial pattern than for the biaxial pattern. However, utilization of the uniaxial pattern in real hardware would compromise seriously the packing density of devices.

This dilemma can be resolved by examining the results within the narrower scope of the preceding design parameter selections of aluminum bonds, 2 - 3 x 10^{-4} inch high, and the 7059 glass substrate. The biaxial pattern used in Cell No. 7 produced a very wide range of strains as is depicted in Figure 17 (d). However, even in the case where the strains approached the theoretical maximum, no electrical failures were detected. Similar related experience is presented in Appendix II. Thus, it might be reasoned that although high strains are not desirable, they can be tolerated in this case so as to avoid compromising the packing density. Thus, it is judged that the biaxial pattern should be selected.

To recapitulate, the assembly design parameters to be used to fabricate specimens for Phase III are:

1. Biaxial bonding pattern

2. Aluminum bonds

3. 7059 glass substrates

4. Bond height of $2 - 3 \times 10^{-4}$ inch.

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PHASE III

EXPERIMENTAL PROCEDURE

1. EXPERIMENTAL DESIGN

In **Phase II, a parametric investigation of various face-bonded assembly** designs resulted in a "practical best" design which was used for this phase of the program. The parameters included bonding pattern, planar circuit material, interconnection material, and interconnection (projection) size.

The results from the Phase II study indicated that the "practical best" assembly design is the one which had been designated as Cell No. 7 in the Phase II study. This design incorporates a biaxial bonding pattern, a 7059 glass substrate, and aluminum projections with an as-bonded column height of $2 - 3 \times 10^{-4}$ inch. In accordance with these recommendations, seven NM 3015 face-bonded devices were fabricated for Phase III. Measurement of the as-bonded bond heights as $2 - 3 \times 10^{-4}$ inch and the shear strength of the assemblies as 300 - 860 grams with a 650 gram average, indicated that the desired duplication of the Phase II, Cell No. 7 assembly design had been accomplished in Phase III. The biaxial bonding pattern, which was used, is shown in **Figure 23.**

In order to evaluate the effect of thermally-induced mechanical strain on the electrical functionality of the devices, the following approach was taken:

Six of the face-bonded devices were strain gaged (see **Figures 24 and 25**) in a manner to measure the strain parallel to the larger edge dimension of the die and perpendicular to the bond lines. In addition, "flying-lead," thermocompression-bonded NM 3015 - glass assemblies (see **Figure 26**) were fabricated, in such a manner that any substrate motion would not induce strains in the device. Five of each type of device were then subjected to a temperature cycle of 25 C to 175 C, while those component parameters which were judged most significant in establishing electrical functionality were monitored. Those parameters included resistance, current gain, junction voltage, saturation voltage, and switching times. The strain gages on the face-bonded assemblies were also monitored at this time. A comparison of the electrical outputs of the two groups of devices would reveal if any deleterious effect on the face-bonded assemblies had been caused by the thermally-induced mechanical strain.

After this comparison was made, the face-bonded devices were subjected to 20 thermal cycles (25 C to 175 C) and monitored for electrical continuity of all bonds.

As an additional check on the integrity of the bonds, a total of three face-bonded assemblies were cross-sectioned and metallographically examined. One device was cross-sectioned after fabrication, one after a single thermal cycle, and one after completion of the 20 thermal cycles.
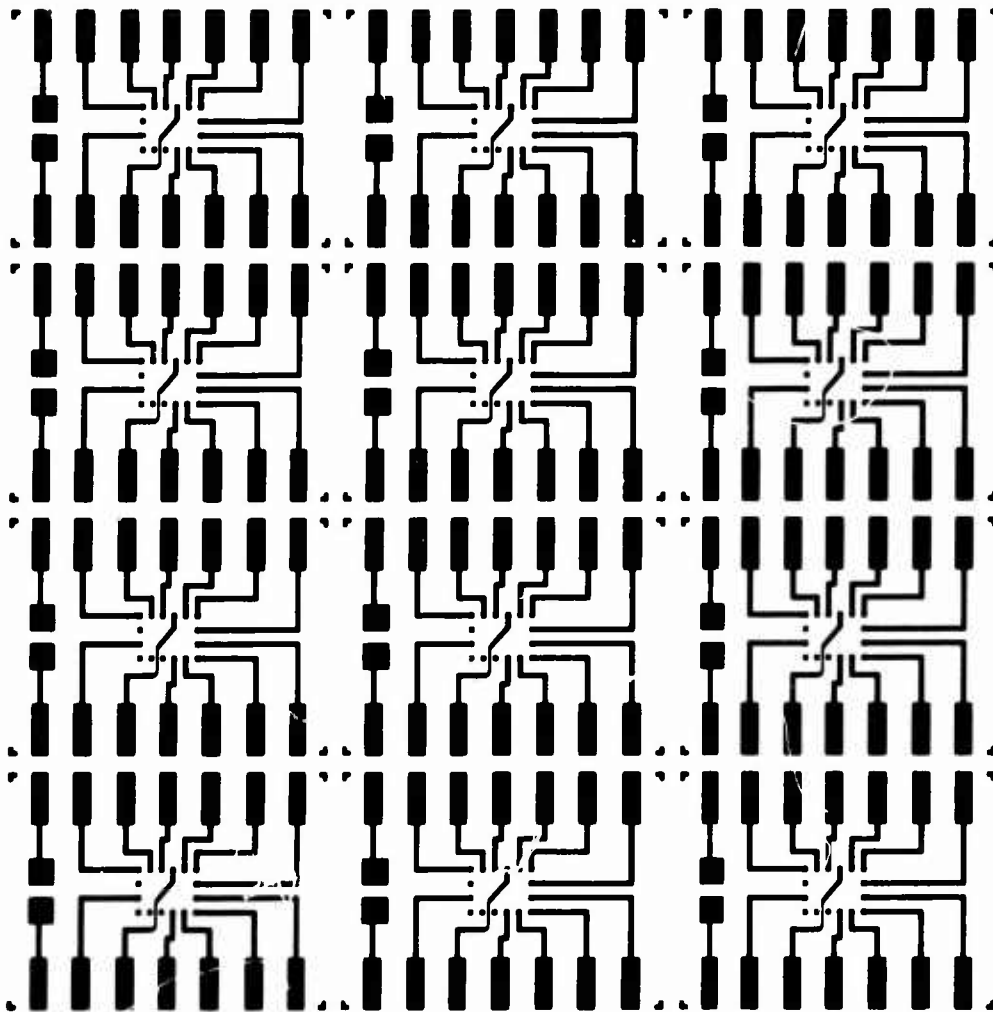
Figure 23. Biaxial Bonding Pattern
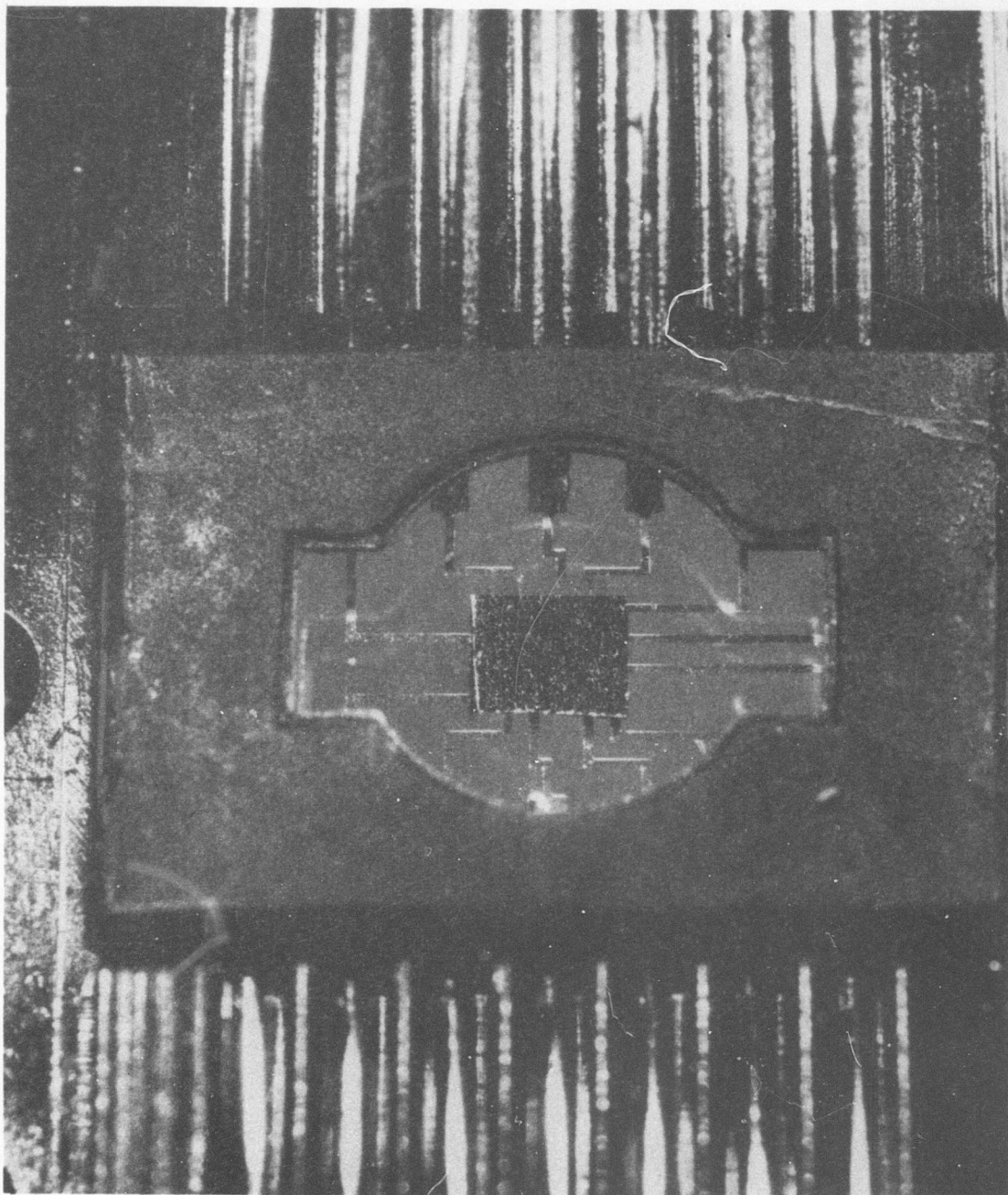
Figure 24. Face-Bonded Assembly

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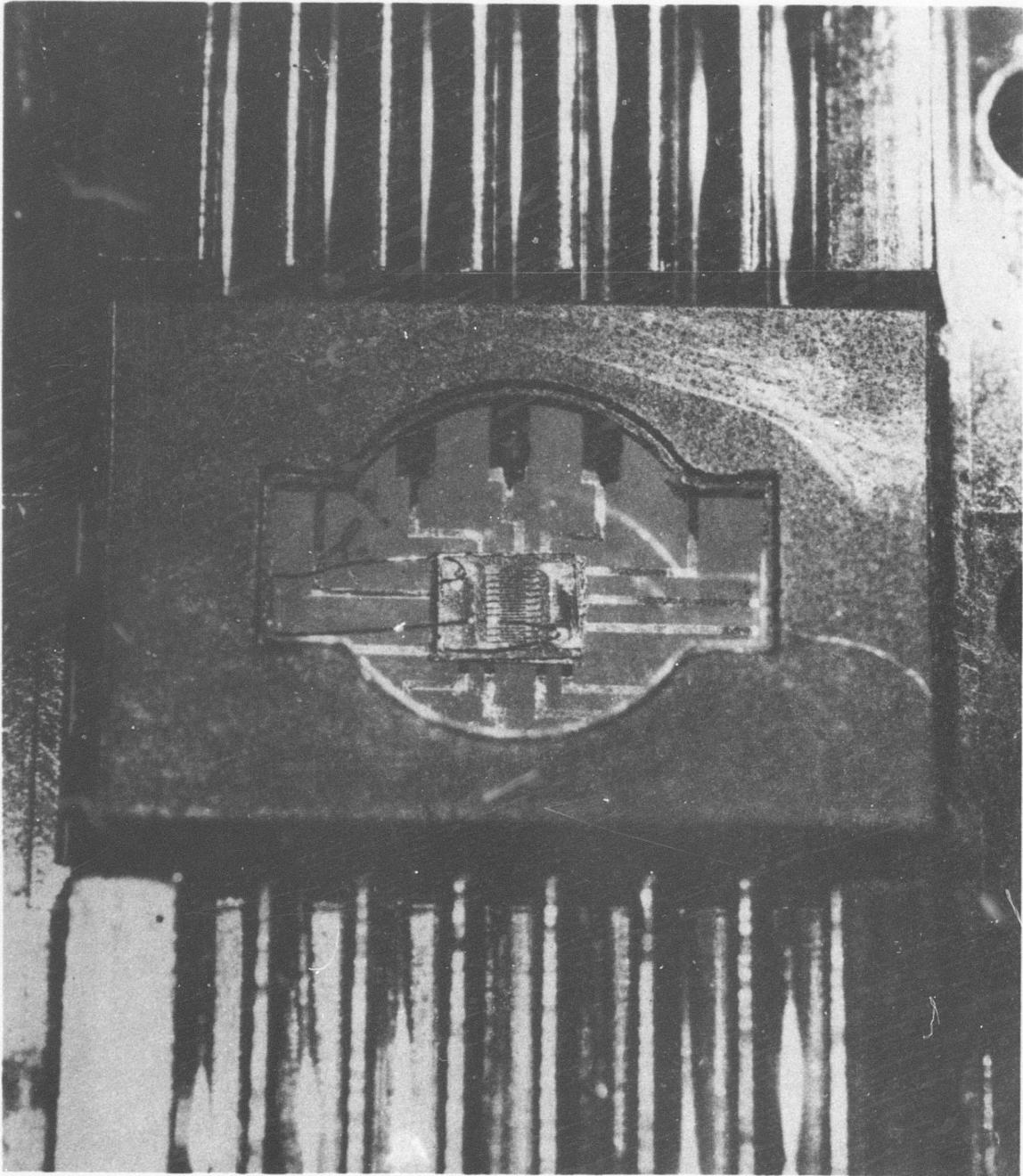
Figure 25. Face-Bonded Assembly With Foil Resistance Strain Gage
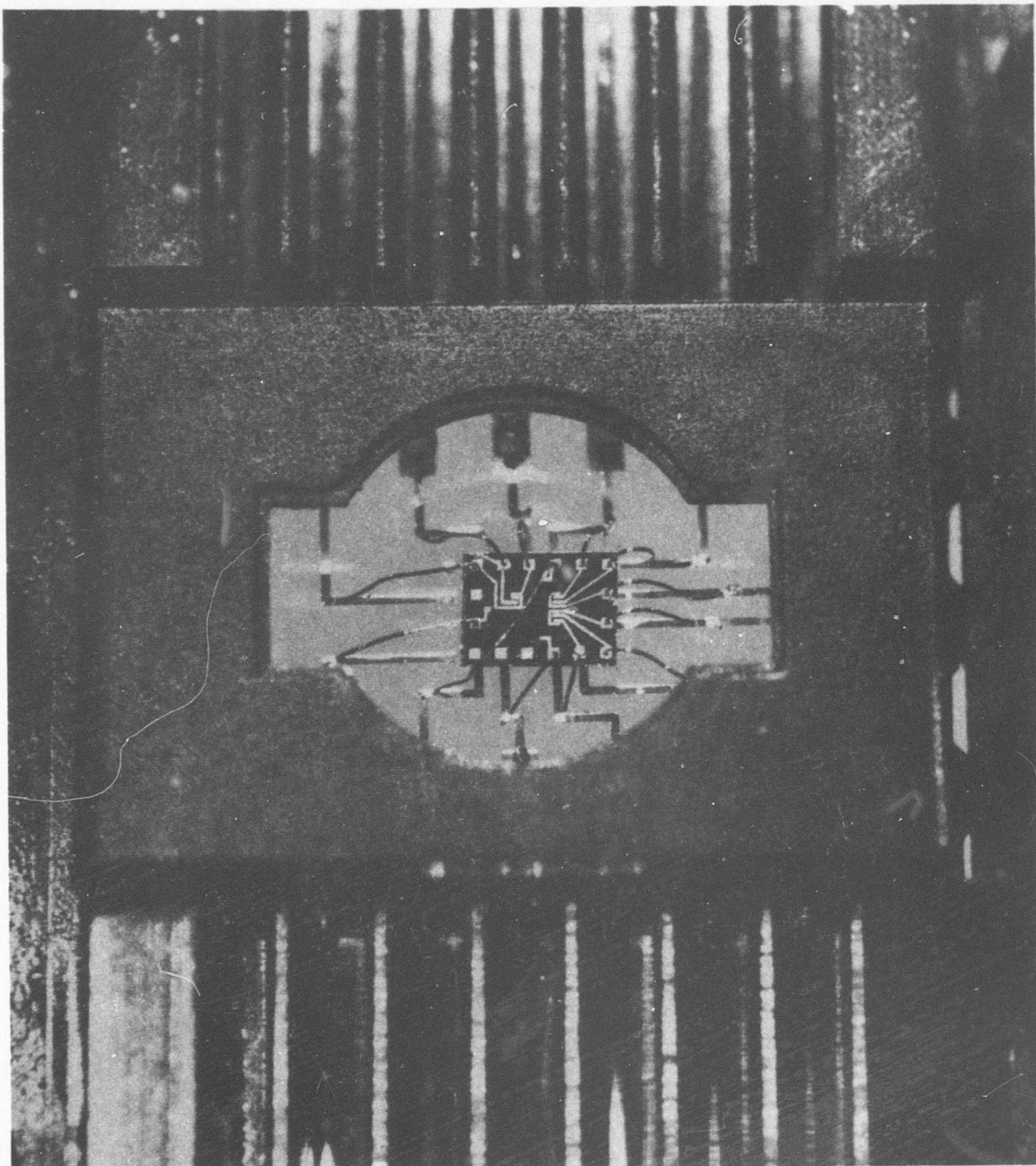
Figure 26. Flying-Lead Assembly

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2. SPECIMEN PREPARATION

A 14 lead flat-pack holder was selected as the container for the circuit to be fabricated for Phase III. The basis for selection of this package was to enable Autonetics to use their standard electrical test equipment. This new package required the use of a new substrate interconnection scheme. The face-bonding technique, the "flying-lead" attachment, and the foil strain gage interconnection were basically the same as were used in Phase II.

The plastic holder required the use of a glass substrate no larger than 0.275 by 0.375 inch. The technique used to obtain the substrates was as follows:

1. A pattern was designed such that the transistors and the resistors would be at pin locations 1 - 14 of the plastic holder as is used by Autonetics in their standard electrical test.

2. The patterns were laid out in a 3X4 array on a 2 x 2 inch glass slide, (Figure 23). The necessary spacing was provided so that a diamond saw could be used to cut the substrates to the desired size.

3. The glass slides were then vacuum deposited with 100 Å of Ni-Cr under 8000 Å of aluminum. The glass itself was Corning 7059.

4. The metallization was then photomasked and etched, resulting in the twelve substrate patterns.

5. The substrates were then cut from the glass slides with a diamond saw.

The next phase of the circuit fabrication that required additional development was the attachment of the output lead wires from the substrate. A microgap bonder was used to join 0.010 inch diameter 99.99 percent pure gold wire to the aluminum metallization on the output pads of the substrates. This technique allows a current to pass through the gold wire while pressure is exerted on the wire toward the aluminum metallization. The current heats the wire and the pressure creates a thermocompression bond beneath each electrode. The wire and the substrate were placed in the plastic holder during this bonding so that accurate positioning could be obtained. In order to verify the capability of the bond to withstand the thermal cycling scheduled for the electrical testing, the following was performed:

A group of gold wires was bonded in a fashion identical to that used in the fabrication of the face-bonded device and then subjected to the same temperatures as were used during the electrical testing. They were initially held at 175 C for one hour and then stored for 24 hours at room temperature. This was done three times and then the bonds were strength-tested. The average strength of the bonds decreased only slightly and thus the interconnection scheme was used to fabricate the circuits.

3. SPECIMEN INSTRUMENTATION

Other than checking the functionality of the electrical components, the only other measurement taken was the thermally-induced mechanical strain. These strain measurements were made using foil-resistance strain gages. The gages were installed with BR600, using a three-wire system. Because of effective utilization of the gaging experience gained in Phase II, no difficulty was encountered in mounting the strain gages.

4. DATA ACQUISITION

After fabrication and strain gaging of the face-bonded devices and fabrication of the flying lead devices, various tests were performed on each group. Electrical functionality versus temperature tests were performed on both groups of devices. Each of the devices was soaked in a small controlled oven while the electrical parameters were recorded at 25, 75, 125, and 175 C. At the same time, thermally-induced mechanical strain was monitored at the same temperatures for the face-bonded devices. A comparison of this data yields the effect of thermally-induced mechanical strain on the electrical functionality of these solid-state devices. The following electrical measurements were made:

1. HFEN (normal beta) at four emitter current levels of 0.03, 0.1, 0.3, and 1.0 ma,

2. HFEI (inverse beta) at four emitter current levels of 0.03, 0.1, 0.3, and 1.0 ma,

3. Vbe (base-emitter voltage), measured at four emitter current levels of 0.03, 0.1, 0.3, and 1.0 ma,

4. Vbc (base-collector voltage), measured at four collector current levels of 0.03, 0.1, 0.3, and 1.0 ma,

5. SV_{ce} (saturation voltage), measured at I_c = 10 ma and I_b = 2 ma,

6. Resistor values,

7. Ratio of the two resistor values,

8. Transistor switching times.

Subsequently, the face-bonded devices were subjected to 20 thermal cycles and monitored for electrical continuity.

Metallographic examinations of the face-bonded joints were made on three face-bonded devices: one after fabrication, one after the electrical functionality tests, and the other after the 20 thermal cycles.

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The strain gages were monitored with a BLH Type 20 strain indicator, the electrical functionality tests with a 7100 A Fairchild Digital Voltmeter, Tektronix 567 sampling scope, and various in-house fabricated test equipment, and the electrical continuity tests with a Triplett Voltohmmeter, Model 630A. The strain indicator had a least count of 2 micro-inches per inch on any strain reading, with an overall accuracy of ⊦ 10 micro-inches per inch on any strain reading, while the overall accuracy of the electronic readout equipment was ± 3 percent.

RESULTS AND DISCUSSION

1. THERMAL STRAIN

Thermally-induced mechanical strain versus temperature tests were run between the temperatures of 25 C and 175 C. The results are presented in Figure 27. The two lines in Figure 27 represent the maximum and minimum values obtained from the five devices. The theoretical maximum line in Figure 27 is taken from the technical report for Phase II. These theoretical maximum values are calculated using the coefficients of linear expansion with temperature for silicon and 7059 glass. The experimental values in Figure 27 exceed the theoretical maximum values because of an additional fixture-induced mechanical strain which was superposed upon the thermally-induced mechanical strain. The bakelite holders which were used to position the face-bonded assemblies during the thermal cycles, were definitely deformed due to heating. The nature of the bending was such, that the additional strain was additive and thus imposed a more severe environment in which the electrical parameters were tested.

2. ELECTRICAL FUNCTIONALITY

Review of the results indicates very little mechanical strain effects on the electrical parameters of the face-bonded devices evaluated. The only apparent effect observed was on transistor gain for very low emitter current, but in general the effects of temperature alone overshadow any measurable effects due to strain. The results of the measurements of the electrical parameters are as follows:

1. HFEN (normal beta):

    This parameter was measured at four emitter current levels of 0.03, 0.1, 0.3, and 1.0 ma. At I_c 0.03 ma and a temperature of 175 C, a difference in ratio of 13 percent is observed. This difference is less at higher current levels and is not apparent at the lower temperatures. These results are presented in Figures 28 and 29.

2. HFEI (inverse beta):

    This parameter was measured at four emitter (collector of inverse transistor) current levels of 0.03, 0.1, 0.3, and 1.0 ma. At I_c = 0.03 ma and a temperature of 175 C, a difference in ratio of 4.8 percent was seen. This difference in ratio is not apparent at higher current levels. These results are presented in Figures 30 and 31.
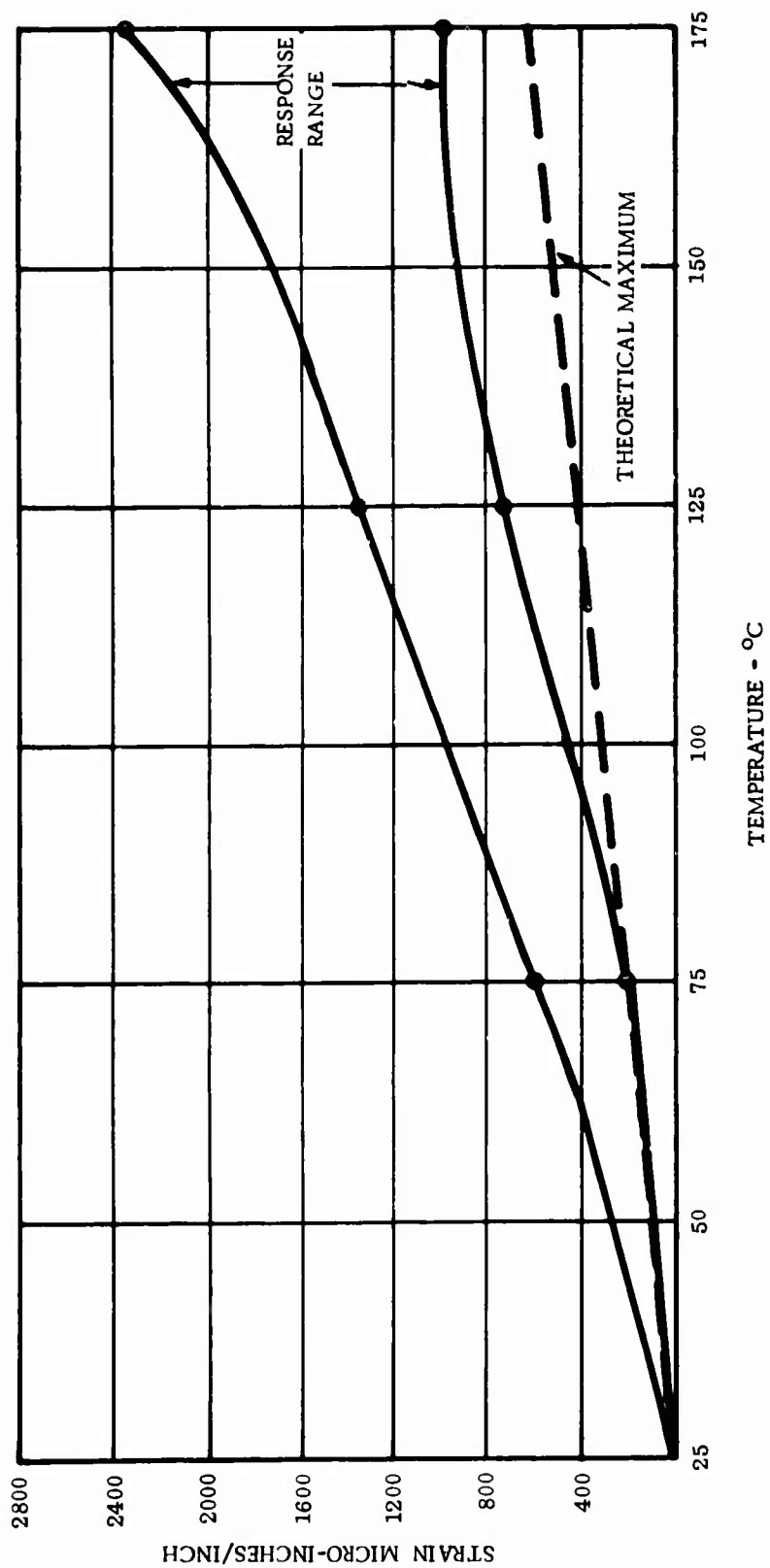
Figure 27. Thermally-Induced Mechanical Strain vs. Temperature

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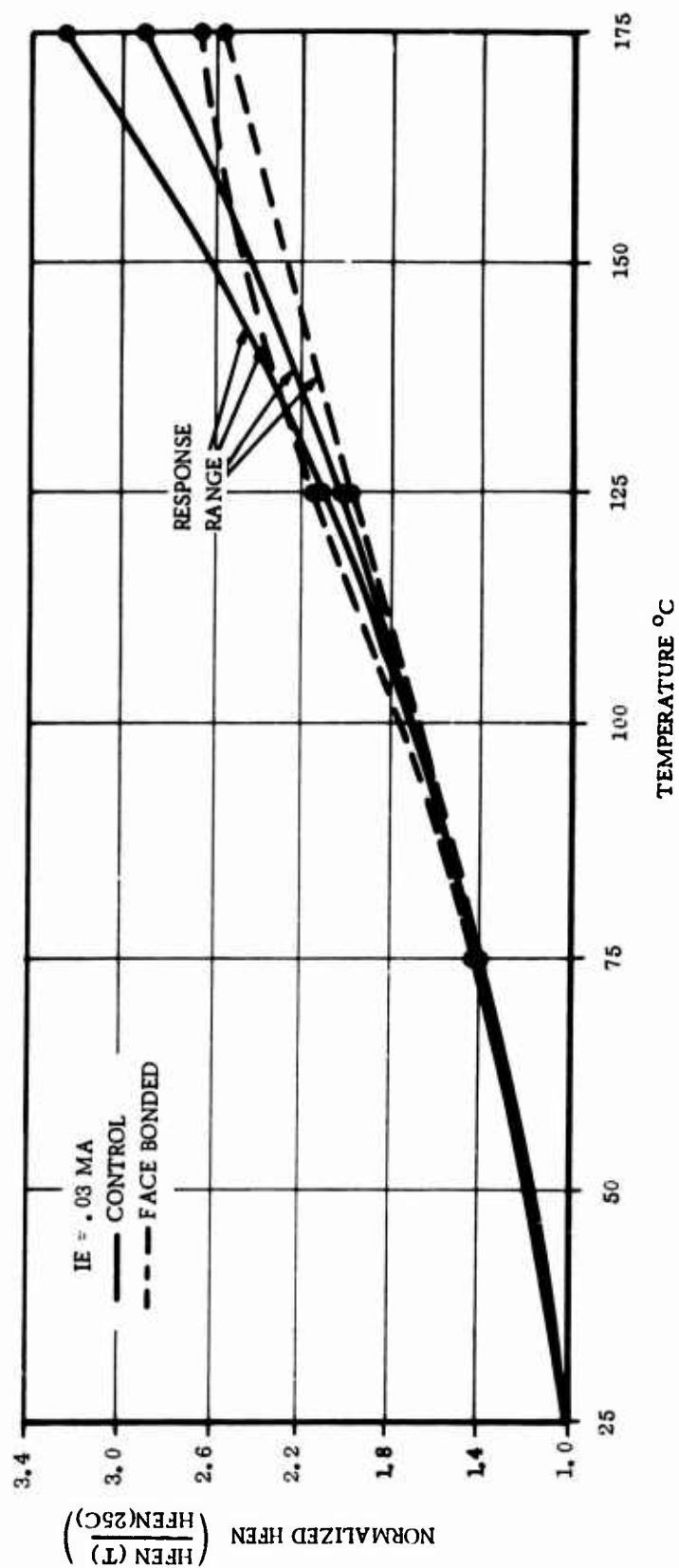
Figure 28. HFEN (Normal Beta) vs. Temperature
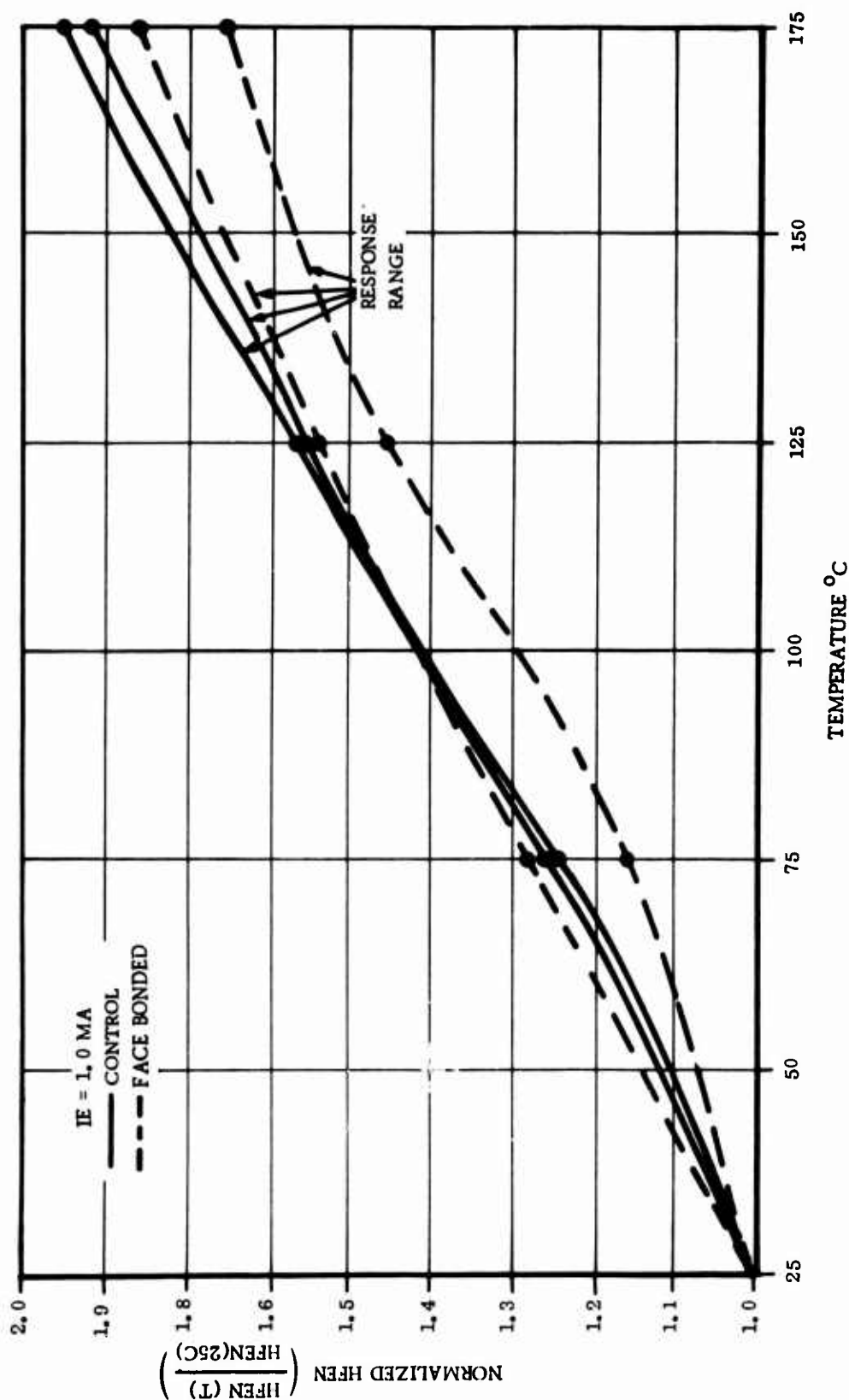
Figure 29. HFEN (Normal Beta) vs. Temperature

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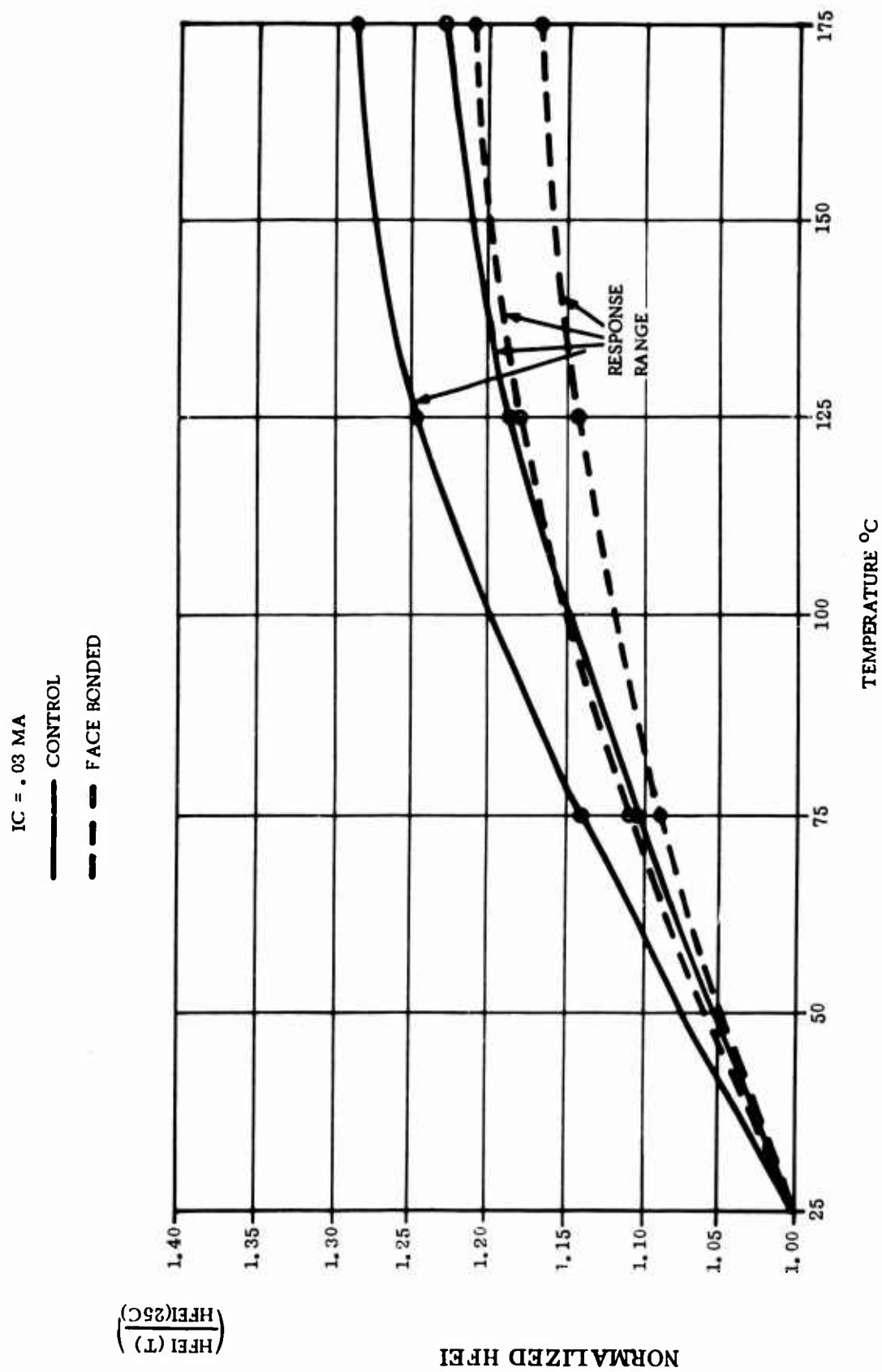
Figure 30. HFEI (Inverse Beta) vs. Temperature
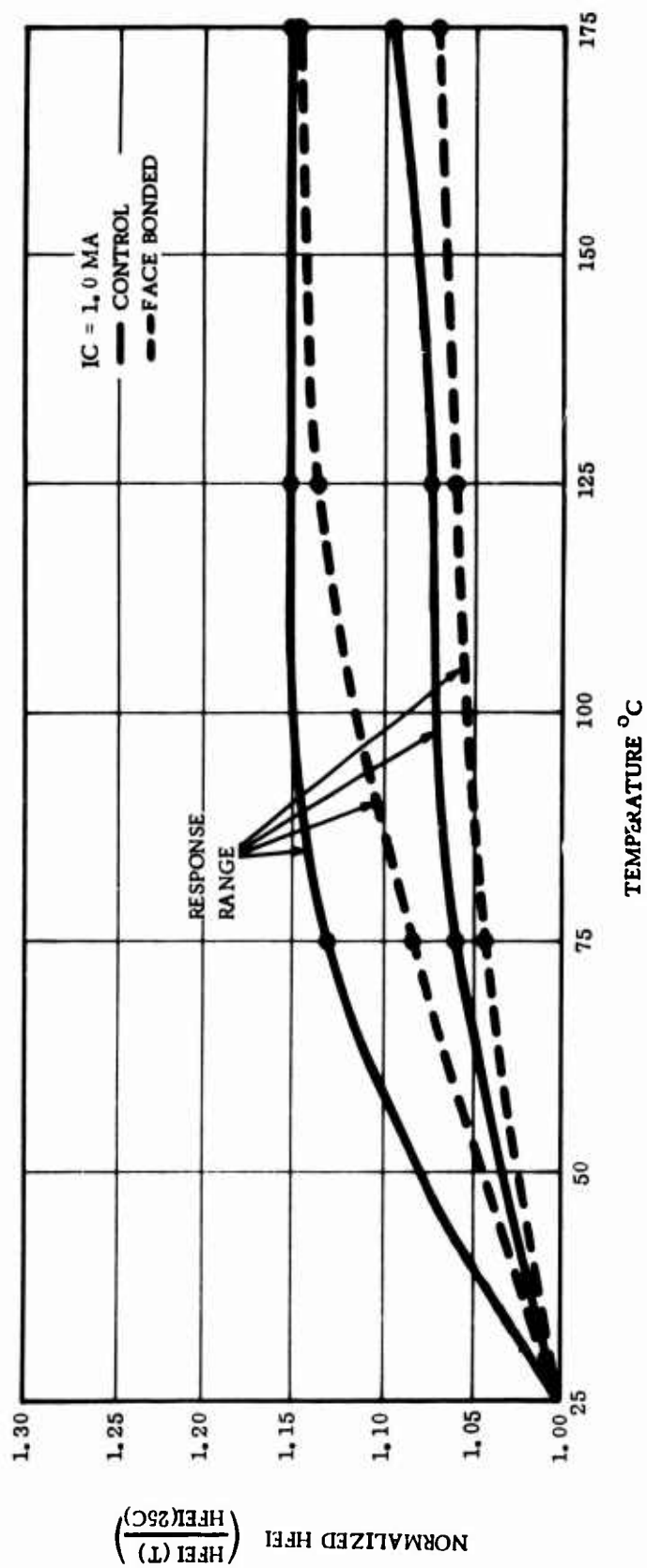
Figure 31. HFEI (Inverse Beta) vs. Temperature

No significant effects due to strain were seen on the following parameters:

1. Vbe (base-emitter voltage):

   This parameter was measured at four emitter current levels of 0.03, 0.1, 0.3 and 1.0 ma, see Figure 32 and 33.

2. Vbc (base-collector voltage):

   This parameter was measured at four collector current levels of 0.03, 0.1, 0.3, and 1.0 ma, see Figure 34 and 35.

3. SV_{ce} (saturation voltage):

   This parameter was measured at a collector current level of 10 ma and a base current level of 2 ma, see Figure 36.

4. Resistor Values:

   See Figure 37.

5. Resistor Ratio:

   Changes in the ratio of the two resistor values were less than 1 percent.

6. Other Parameters:

   In addition to the foregoing, the breakdown voltages BV_{CEO}, BV_{CBO} and BV_{EBO}, the substrate bulk resistance, and switching times (measured as defined in Figure 38) were similarly unaffected by thermally-induced mechanical strain.

3. METALLOGRAPHIC ANALYSIS

Typical photographs of the metallographic sections of face-bonds are presented in Figures 39 through 42. Figure 39 pertains to the device which was sectioned after fabrication, Figure 40 to that which was sectioned after a single thermal cycle during which the functionality of the electrical parameters was monitored, and Figures 41 and 42 to that which was sectioned after 20 thermal cycles during which the electrical continuity was monitored.

The bonds for the device which did not undergo thermal cycles (Figure 39) appear to be of excellent quality. The upper photograph shows an almost perfect bond and the other shows a good bond, however a slight cone-conductor interface is visible at the outer edges of the upset material.
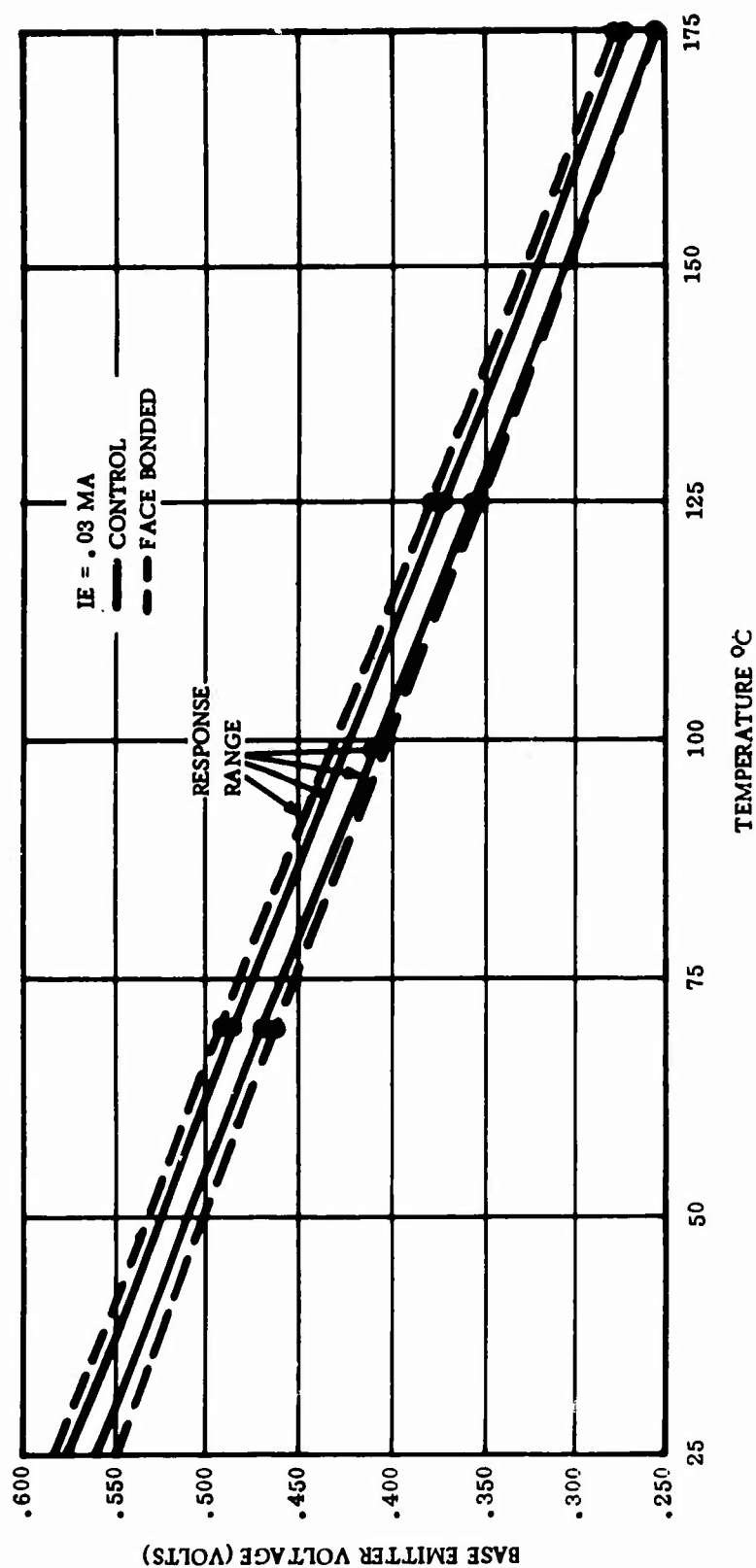
Figure 32. V_{be} (Base Emitter Voltage) vs. Temperature

78
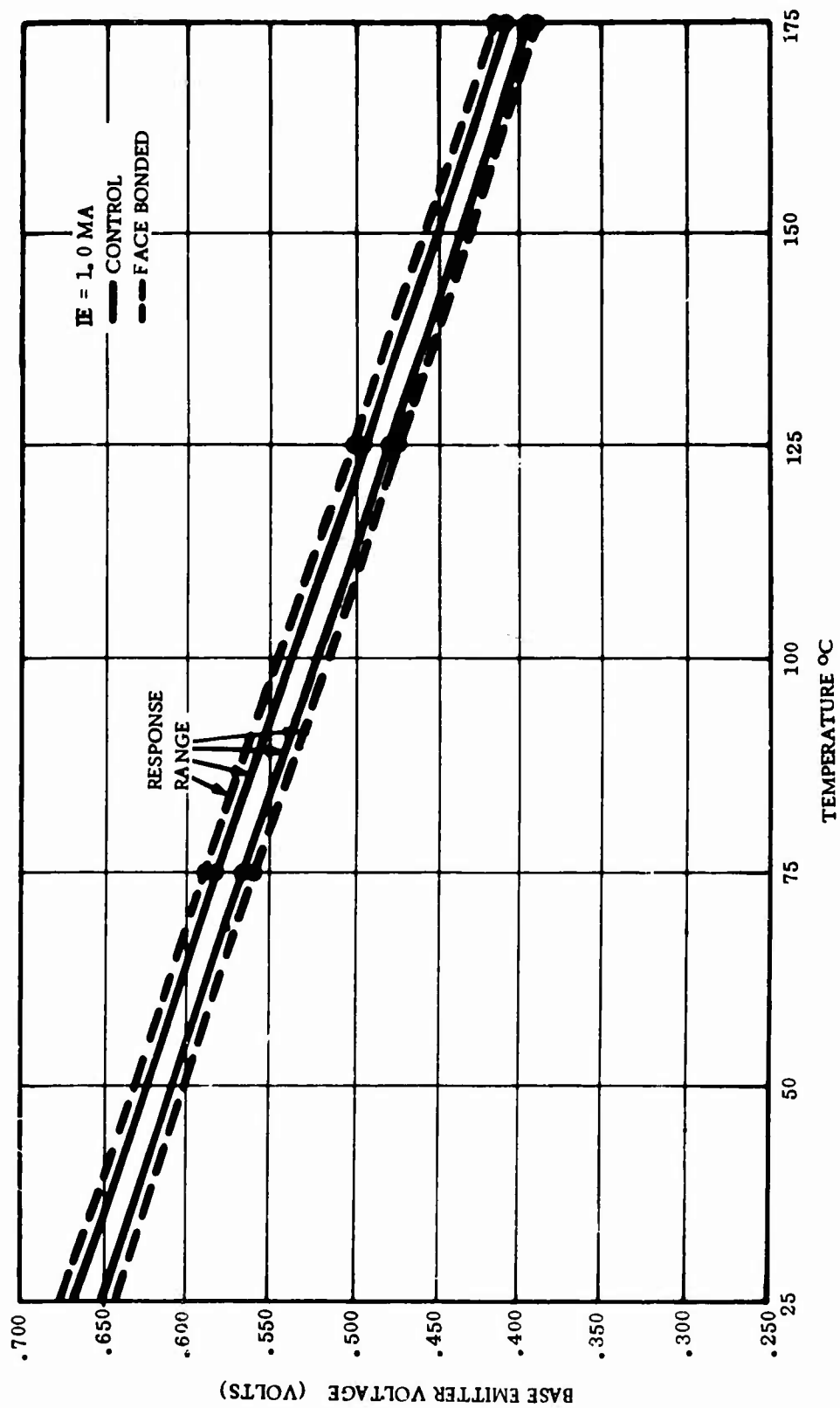
Figure 33. V_{be} (Base Emitter Voltage) vs. Temperature
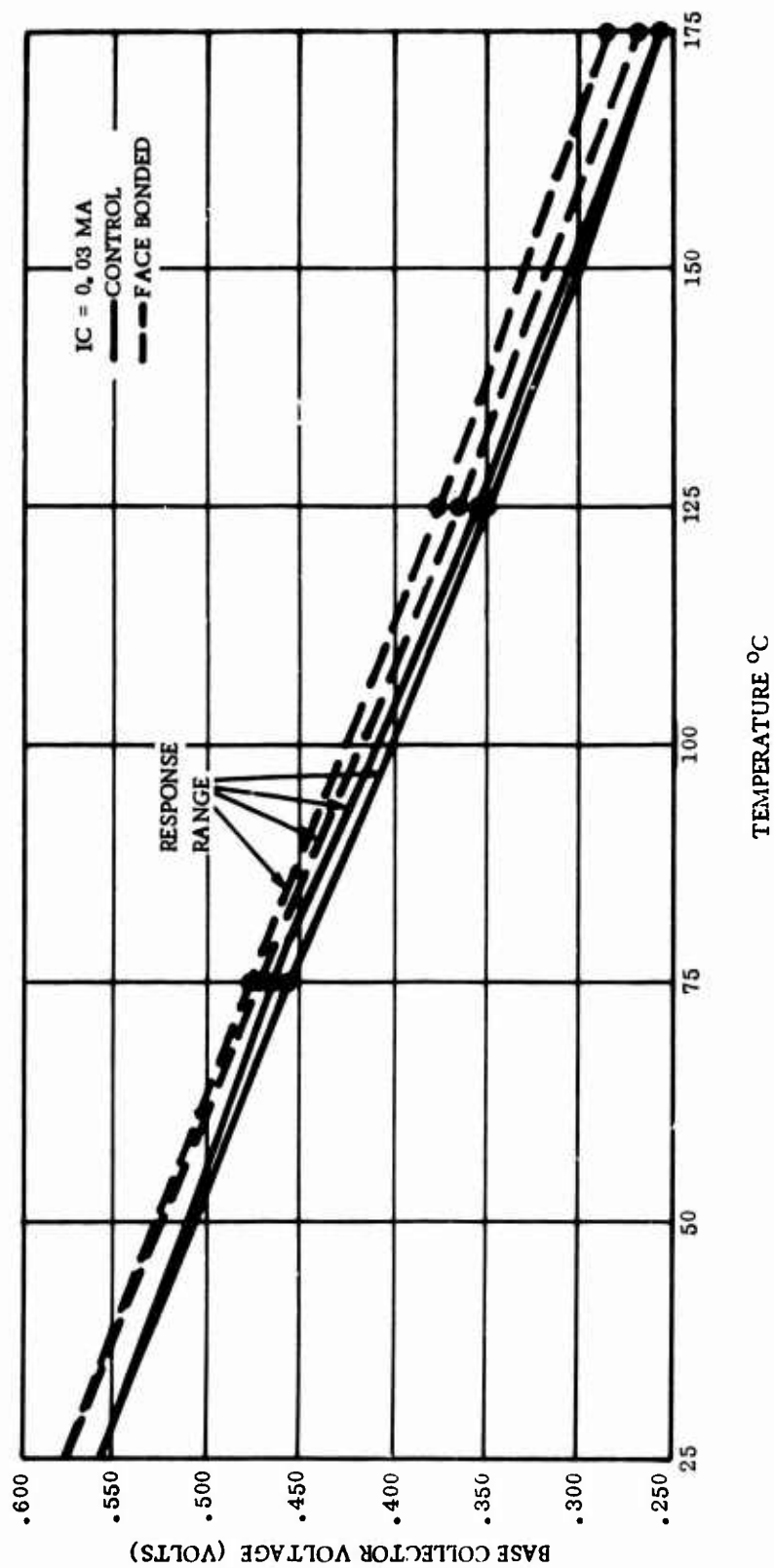
Figure 34. V_{bc} (Base Collector Voltage) vs. Temperature

80
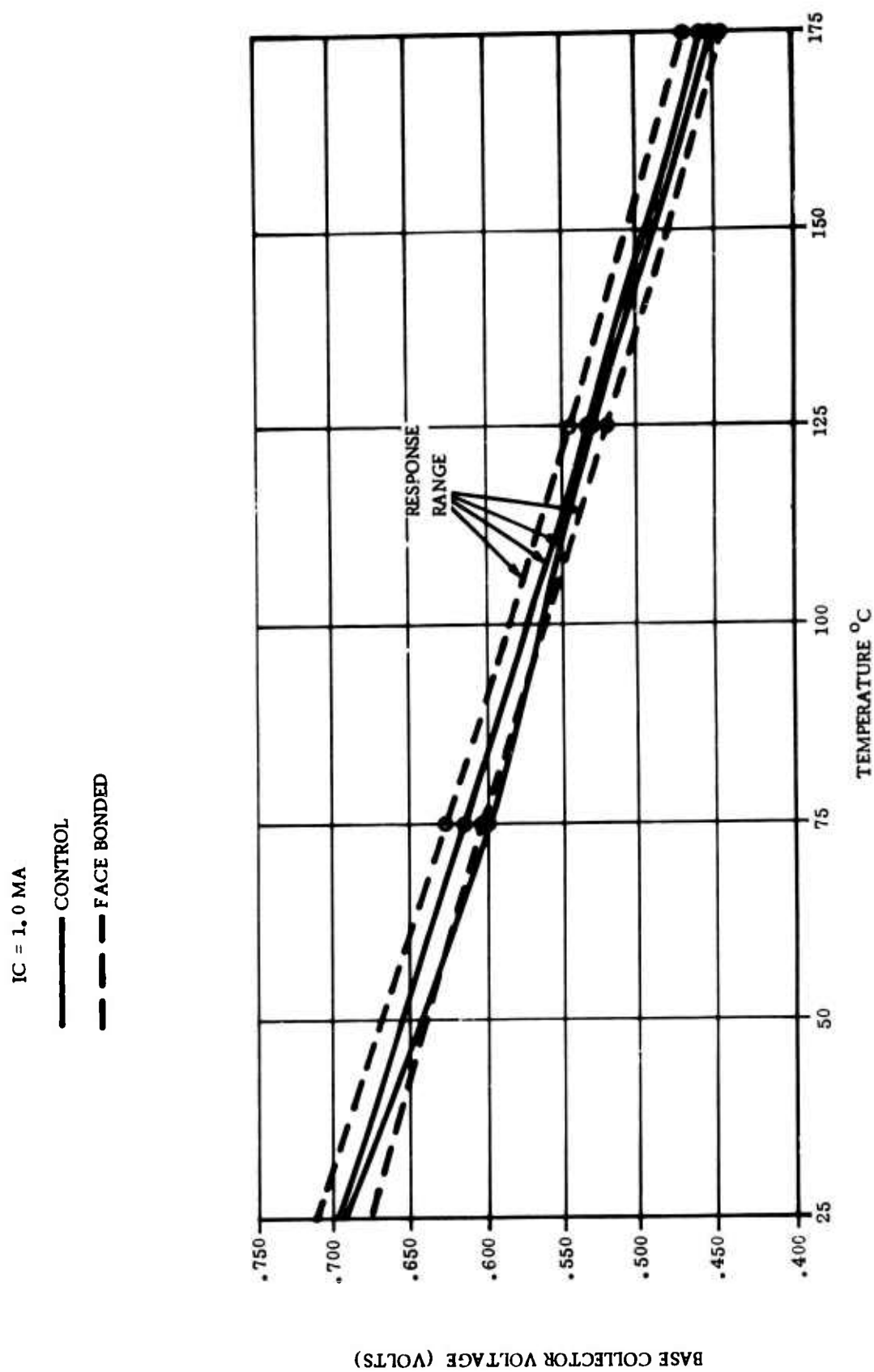
Figure 35. V_{bc} (Base Collector Voltage) vs. Temperature

81
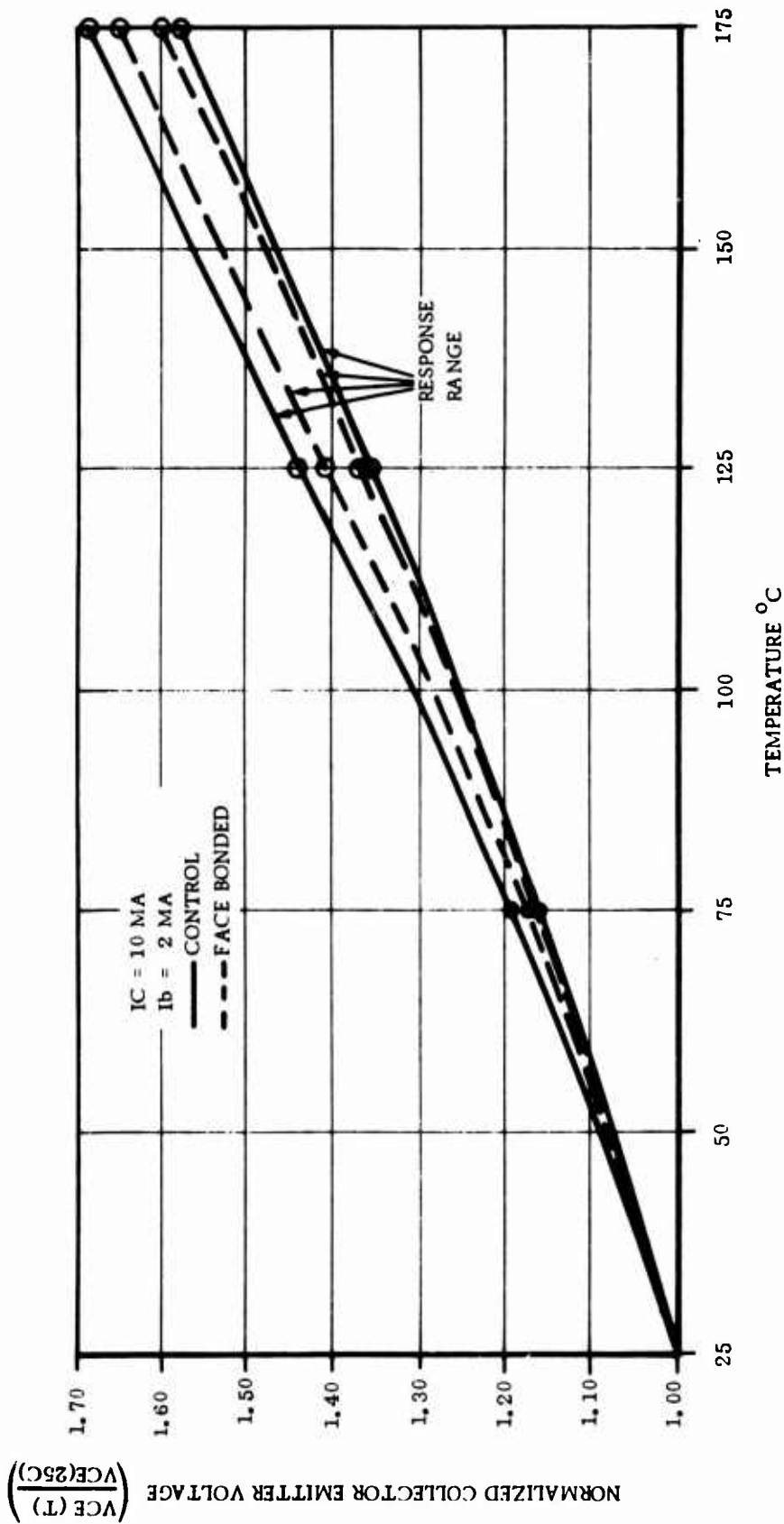
Figure 36. SV_{ce} (Collector Emitter Voltage) vs. Temperature

82
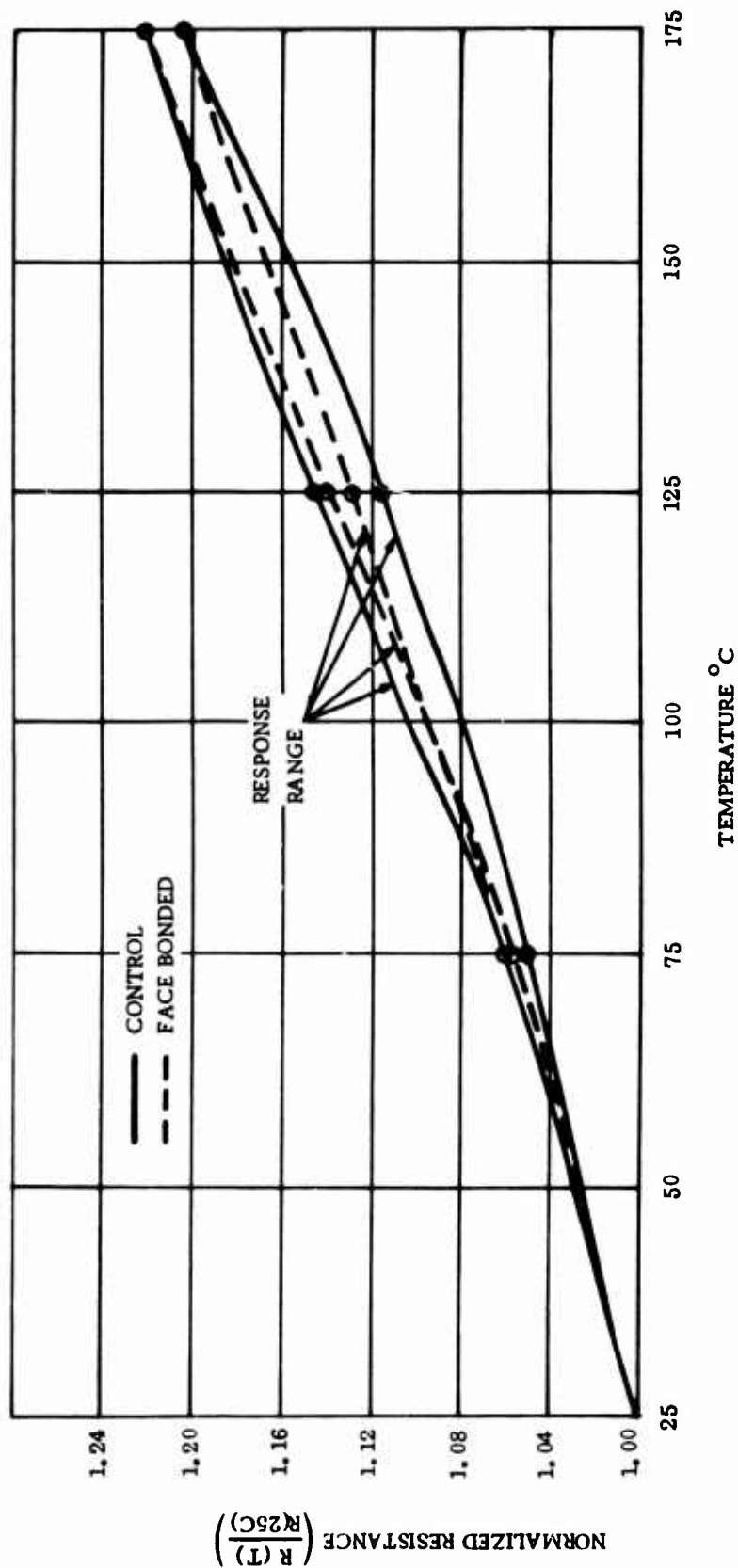
Figure 37. Resistance vs. Temperature

83
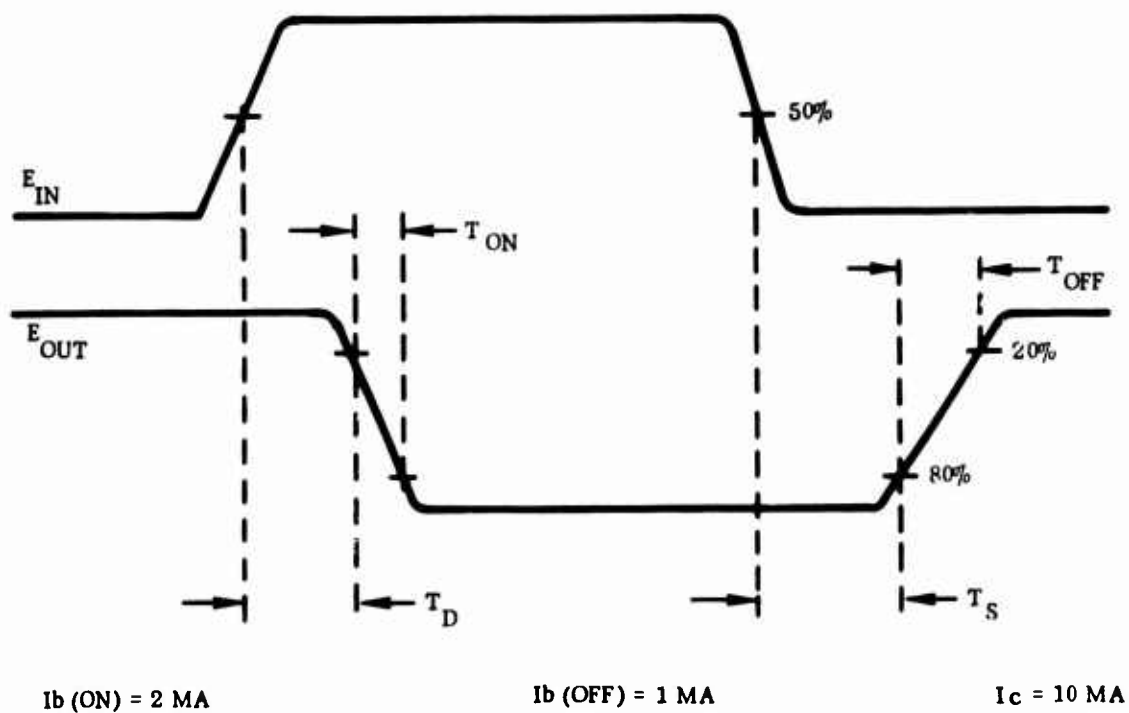
Figure 38. Transistor Switching Times
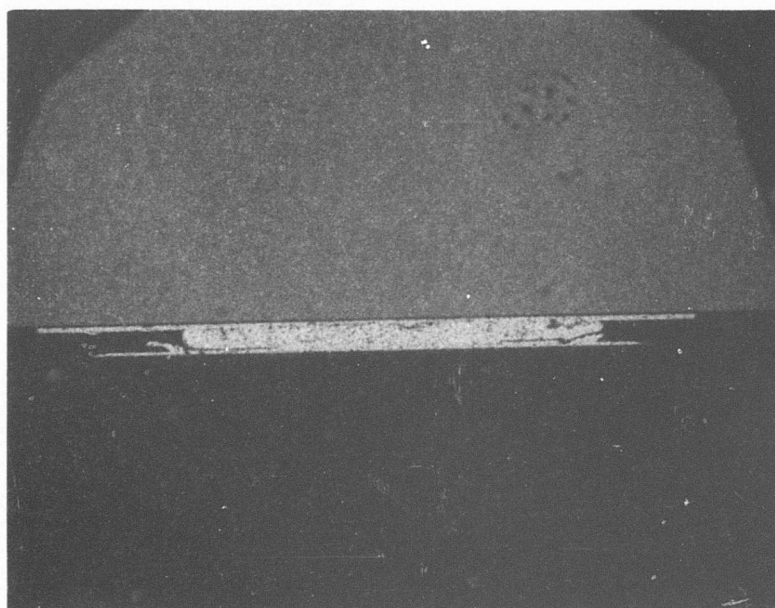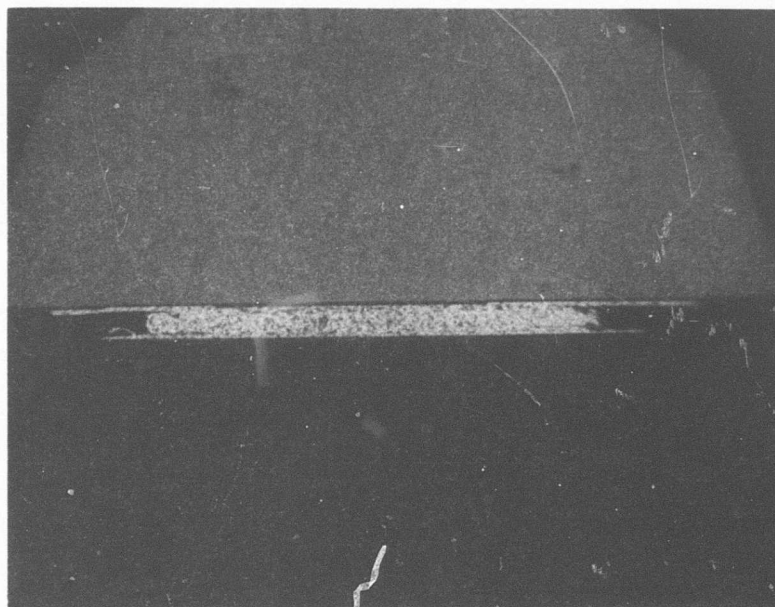
Figure 39. Metallographic Sections of Face Bonds
No Thermal Cycles. (Keller's Etch–630X)

85
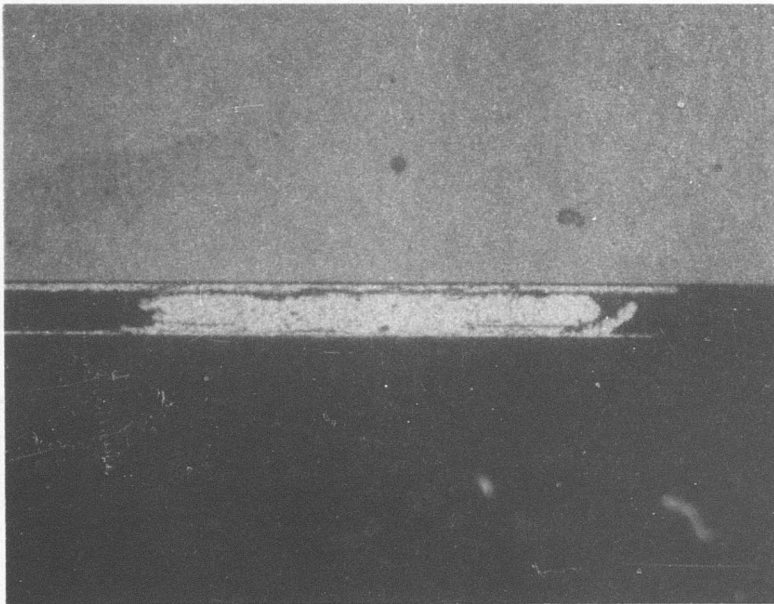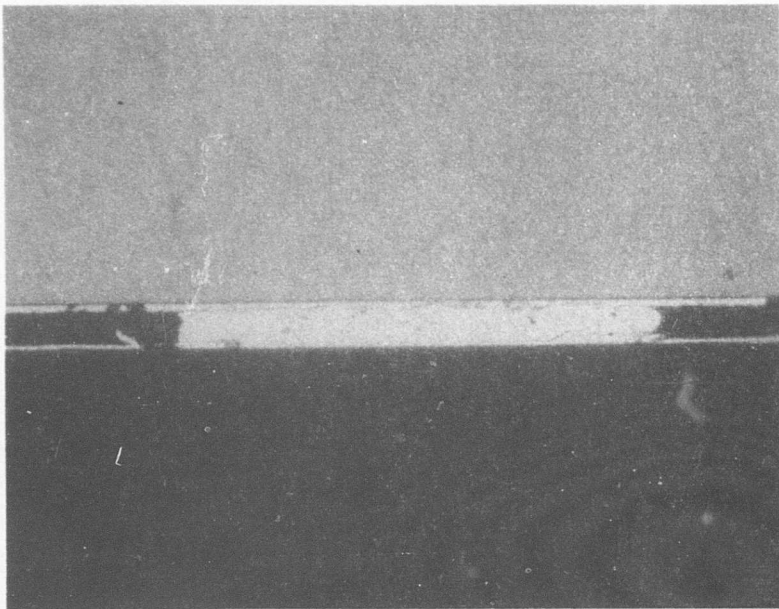
Figure 40. Metallographic Sections of Face Bonds
After One Thermal Cycle. (Keller's Etch-750X)
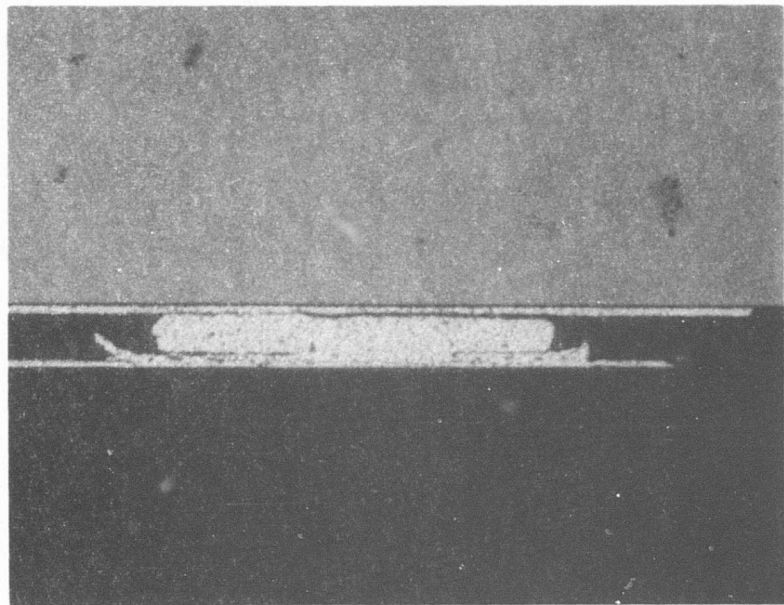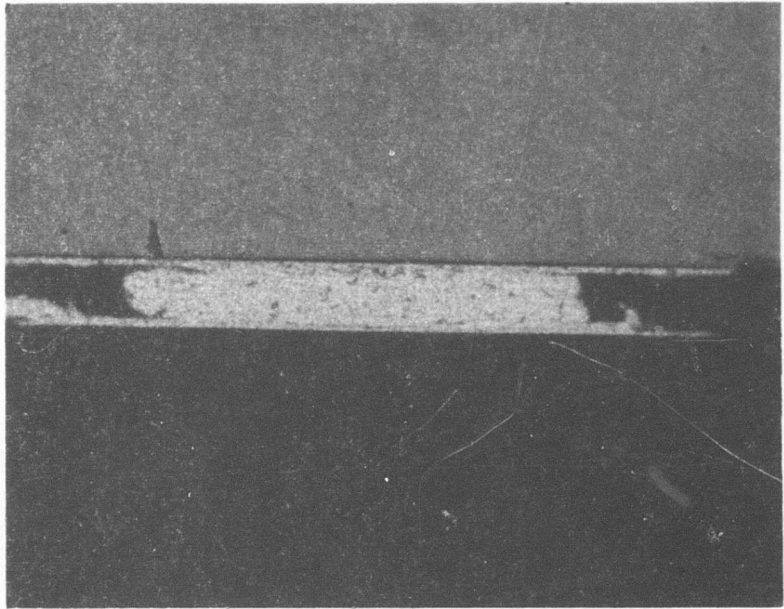
Figure 41. Metallographic Sections of Face Bonds
After 20 Thermal Cycles. (Keller's Etch–800X)
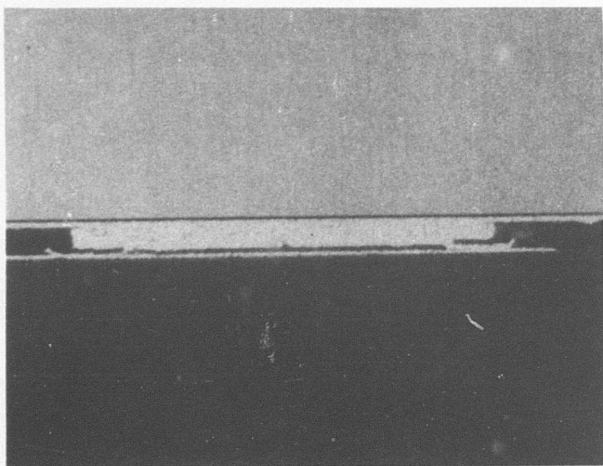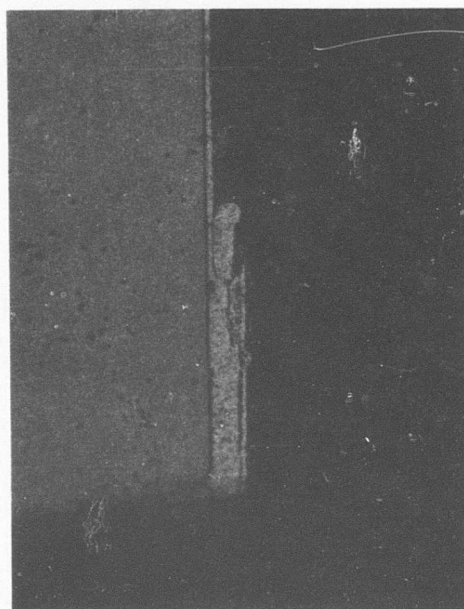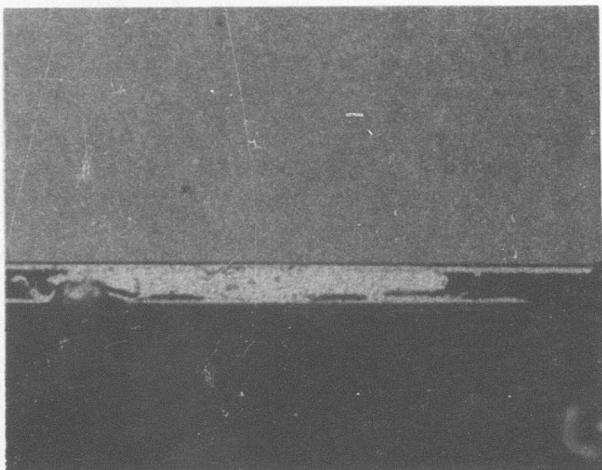
Figure 42. Metallographic Sections of Face Bonds
After 20 Thermal Cycles. (Keller's Etch-800X)

The bonds for the device which had seen one thermal cycle (Figure 40) are also of good quality. The section in the lower photograph of Figure 40 appears to have a discontinuity between the bond and the metallized pad on the silicon. However, as is more apparent in Figures 41 and 42, the bond has taken on a slight "S" shape and this particular cross-section was taken perpendicular to the "S" shape at a point where it dips away from the silicon.

In Figure 42, the upper left photograph is a cross-section perpendicular to the "S" shape. The lower left photograph shows a second plane, deeper in the same bond and parallel to the first plane. The photograph on the right contains the "S" shape, which is perpendicular to the two cross-sections. Again, the apparent discontinuity, this time between the bond and glass, emphasizes the "S" nature of the bond. The bond on the right is so short because it has been taken after the first two sections were made. Again it should be emphasized that, although a "breathing" action may have taken place in the assemblies that were subjected to thermal cycling, electrical continuity was maintained at all times. These observations were consistent with those reported in the Phase II technical report.

CONCLUSIONS

The primary objective of Phase III was to determine the effects of thermally-induced mechanical strain on the electrical functionality of a typical solid-state device. These typical solid-state devices were fabricated in a manner selected as the "practical best" design in Phase II of this program.

Another objective of the program was to monitor the electrical continuity of the face-bonds during 20 thermal cycles.

The objectives of Phase III have been fulfilled and the results have shown that for the most part, the electrical performances of the components mounted on the face-bonded NM 3015 assemblies were not affected by thermally-induced mechanical strains. In the two cases where there were slight effects, these effects were overshadowed by the effects of temperature alone. Thus, it can be concluded that the face-bonding techniques employed should cause no appreciable effects on integrated circuit electrical performance from 25 to 175 C, under the conditions tested.

The face-bonded devices were also able to maintain their electrical continuity throughout 20 thermal cycles. This was verified not only by monitoring the electrical continuity with an ohmmeter, but also by the metallographic analysis of samples.

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APPENDIX I

Electrograph Method for Locating Pinholes in Thin Silicon Dioxide Films

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The electrochemical procedure (1) described in this paper enables simple nondestructive determinations of the precise location of pinholes or other oxide anomalies in thin dielectric material that has been superimposed on and is in contact with a conductive substrate base. The basic principles of the method were first disclosed in a presentation by Besser and Meinhard (2). The particular application presently described relates specifically to a technique used for locating oxide anomalies in thermally grown silicon dioxide passivation layers formed on both phosphorus and boron doped silicon wafers. A need exists in the industry for locating the surface defects at an early stage in production, since electrical failures subsequently occur when vacuum deposited interconnects placed over the holes are short circuited to the conductive substrate beneath. If the faulty areas could be located in the early processing stages, great cost savings and improved reliability would be realized.

An apparatus and technique for carrying out the electrograph method is given in detail in Scott (3). This apparatus could very well be used to advantage for the present application if a sensitive pressure gauge were included to permit accurate control of contact pressure and thereby prevent possible damage to the wafers. The objective of the method, as described in (3), is to obtain qualitative identification of surface components by anodic dissolution in order to chemically transfer small amounts of the surface elements to a suitable medium, usually paper. Distinctive color reactions then occur at specific areas reflecting the compositional differences in the surface. The present electrograph method, however, utilizes a different principle in that a colorless organic reagent, namely benzidine, is anodically oxidized to a colored product only at conductive sites, and does not form a colored compound with any reacting species dissolved from the surface. Since conductive sites represent areas of exposed substrate, the method is conveniently applied to the location of holes in passivation layers.

Experimental

Apparatus.—The apparatus used (see Fig. 1) consists of an electrochemical cell using an aqueous acidified solution of benzidine hydrochloride as an electrolyte. The cell is provided with a supporting stainless steel cathode, 1.5 in. in diameter by 1.5 in. high or slightly wider than the 1.25 in. silicon wafers electrographed,
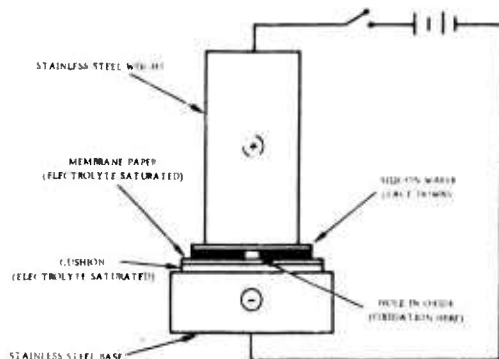
and an anode of the same material, 1.0 in. in diameter by 6 in. in length, or slightly smaller in diameter than the wafers. As a support pad, a soft cloth such as felt, velvet, certain broadcloths and the like, proved satisfactory. Plain white "Millipore" membrane filter papers were used for recording the electrographs. The 47 mm diameter papers with a 0.45μ pore size furnished excellent results for the 1.25 in. silicon wafers.

Procedure.—Cover the top of the cathode base of the electrograph assembly with a soft cloth pad. Add the benzidine-hydrochloride electrolyte dropwise to the pad until it is completely saturated with the reagent. Immediately place a suitable size membrane filter paper saturated with the electrolyte on top of the pad. The membrane paper may be conveniently saturated by immersing it in a small petri dish containing the electrolyte. Add a few drops of electrolyte to the paper after placing it on the pad to ensure complete saturation. Immediately place the silicon wafer, oxide surface down, on top of the membrane paper. The oxide layer of the wafer should have previously been degassed by immersing, oxide surface up, in a petri dish containing sufficient electrolyte to cover the wafer, and evacuating for 5 min or longer under a vacuum of at least 20 mm of mercury. The evacuation step removes entrapped air from pinholes in the oxide and fills them with electrolyte. Place the anode rod on top of the conductive side of the wafer. Remove all excess electrolyte from around the anode base using an absorbent paper, such as a "Millipore" pad. If the excess electrolyte is not removed, it will tend to cause external short circuits around the wafer. Apply sufficient potential to produce a current of about 1 ma (usually about 5 to 10v) at the start, and maintain at this voltage for 5 to 10 min. Turn off the power supply, disassemble the apparatus, then remove the membrane paper for microscopic examination. Open areas in the oxide will be replicated on the paper with black markings or patterns corresponding exactly in size and shape to a mirror image of the conductive areas present in the wafer.

If repetitive electrographs are to be made of the same wafer, place the previously electrographed wafer in a large plastic beaker cover, preferably Teflon. Cover the wafer with a few ml of 6N HCl and allow 2 to 3 min for reaction. Rinse well with pure water to remove most of the benzidine hydrochloride. Repeat this operation once more. Cover the wafer with a few ml of 0.5% HF etchant and allow to react for exactly 1 min. This treatment removes about 25A of silicon dioxide in this time period and should be sufficient to remove all of the oxide formed during the electrographing process. Rinse well with pure water to remove the etchant and reaction products. The wafer is now ready for producing another electrograph. If, however, the wafer is now to be returned to the production line, the final pure water rinse must be of 18 megohm or better quality.

Preparation of Reagents

Benzidine-hydrochloride electrolyte.—To a small beaker add 50 ml of pure water, 10 ml of concentrated hydrochloric acid, and 10g of ACS grade benzidine. Warm on a hot plate until completely dissolved. In another beaker prepare a 5% solution by adding 5g of

Fig. 1. Electrograph assembly diagram

Fig. 2. Electrograph of silicon wafer containing etched micro-circuitry patterns.

Fig. 3. One of individual integrated circuits of the electrograph of Fig. 2 showing pinhole location.

Fig. 4. Replica electron micrograph of oxide anomaly located by means of the electrograph method.

gelatin to 100 ml of boiling water. Boil for 3-5 min. Combine and mix the contents of the two beakers. Filter through a Whatman No. 40 filter paper into a one liter dark glass bottle. Dilute the filtrate to approximately one liter. Stopper bottle then invert to mix well. The reagent may be used for long periods of time if filtered each time before use.

Hydrofluoric acid etchant.—Prepare an approximately 0.5% hydrofluoric acid etchant solution by diluting 10 ml of 48% hydrofluoric acid to about one liter with pure water in a plastic bottle.

Discussion

Benzidine in acid solution can be oxidized electrochemically to a blue oxidation product (4), in accordance with the following chemical reaction

Fig. 5. Etching of silicon dioxide with 0.5% hydrofluoric acid

The above sensitive reaction is the basis of the electrochemical method described in this paper.

The simplified drawing of Fig. 1 illustrates the principle of the technique as applied to the determination of the location of conductive areas or holes through the silicon dioxide dielectric of silicon wafers. When a suitable anodic potential is applied to the silicon wafer, oxidation of the colorless benzidine occurs only at conducting areas such as at unwanted pinholes, etched microcircuitry and the like. The dark blue to black oxidation product formed at the conductive sites produces markings or patterns on the paper having the same size, shape, and location as a mirror image of the conductive areas of the wafer electrographed.

Figure 2 is a photograph of an electrograph prepared on a "Millipore" type membrane paper. The silicon wafer electrographed contained 280 complete integrated circuits etched into the silicon dioxide passivation layer. It will be noted that the uniformity of the pattern is broken in two areas, one to the right of center and the other in the upper left hand area. Successive electrographs duplicated the same incomplete pattern in the identical areas. The broken pattern areas represent faulty etching of the microcircuitry patterns in the oxide produced during processing of the wafer. A faulty circuitry pattern, pinhole or other oxide anomaly recorded on an electrographed membrane is not considered as such until it has been duplicated at least once.

Figure 3 is a photomicrograph (50X) of one of the individual integrated circuits selected from the electrograph shown in Fig. 2. The pinhole designated by an arrow illustrates the appearance of an oxide anomaly of this type when observed by microscopic examination of an electrograph.

Figure 4 is an electron micrograph replica of an oxide anomaly on an actual wafer magnified 5000 diameters. The anomaly on the wafer was located by means of the electrograph shown in Fig. 3.

During the course of the development of the electrolyte for the process, the benzidine was first dissolved in a slight excess of acetic acid. It was later discovered that when hydrochloric acid was substituted for the dissolution of the benzidine, a dark blue to black pattern was achieved instead of the light blue color resulting with the former acid. To further improve on the quality of the electrograph produced, a protective colloid such as gelatin was incorporated into the electrolyte to inhibit crystallization of the benzidine and thereby enhance the definition obtained.

Successive Electrographs

When a silicon wafer is electrographed, it is made the anode of an electrochemical cell and therefore some anodic oxidation of the exposed silicon occurs. If a second electrograph of the same wafer is attempted, no dark areas will form on the membrane paper since the formerly conductive sites are now covered with a thin oxide film. Chemical tests indicate that this developed oxide has an approximate thickness of about 25A. In order that successive electrographs may be processed on the same wafer, a mild etchant was developed which would remove this ultra-thin oxide without serious attack of the main passivation layer. The etchant found suitable was an aqueous 0.5% hydrofluoric acid solution. Figure 5 shows the relationship between the thickness of silicon dioxide removed by the acid per unit contact time. It will be noted that the etching rate was linear in the time interval studied. The data for preparing the graph were obtained by treating a wafer having a silicon dioxide passivation layer of approximately 8500A thickness, with sufficient etchant to just cover the oxide layer side for successive 1 min intervals. The amount of dissolved silicon in the etchant was then determined by a spectrophotometric chemical procedure developed for this purpose. The thickness of the oxide removed was then calculated from the micrograms of silicon dissolved in the etchant, the measured surface area in square centimeters and an assumed density of 2.15 for the silicon dioxide.

Summary

A simple nondestructive electrograph procedure has been developed for locating pinholes or other oxide anomalies in silicon dioxide passivation layers of silicon wafers. The method is most suitable for the determination of oxide anomalies in silicon wafers that contain etched patterns, such as for microcircuitry, which serve as reference guide lines in establishing the precise coordinates of the defects in the passivation layer. It is estimated that pinholes as small as 1000A in diameter can be located by the method.

The electrograph procedure described should find applicability in the determination of surface defects in any thin dielectric material that is superimposed on and is in contact with a conductive substrate base. For example, it should be possible to determine surface defects in silicon nitride dielectric over silicon, germanium oxide over germanium, aluminum oxide over aluminum, and many others.

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APPENDIX II

THERMAL CYCLE STRAIN TEST OF ULTRASONICALLY FACE-BONDED SILICON CHIPS

1. INTRODUCTION

An ultrasonic face-bonding effort in addition to the contracted program was performed for Phase II of the RADC contract, at the request of M. H. Bester, Manager, Department 548, Autonetics. The purpose was to obtain a preliminary indication of the reliability of face-bonded silicon dice attached to 7059 glass in a typical thermal-mechanical environment. Such data would anticipate bond reliability problems prior to major phases of RADC effort.

The face bonding and electrical continuity testing was performed by this group, and thermal cycling and shear stress calculations by the Mechanical Metallurgy Group of the Materials and Processes Laboratories. This report describes the testing, calculations, and the results of the investigation.

2. CONCLUSIONS

Bond strengths of the interconnections between the 36 silicon dice and the Corning 7059 glass substrates were not significantly affected by the thermal cycle testing. The two dice that did indicate a failure were bonded using parameters that produced the lowest shear strength. Both of these dice were bonded at the schedule incorporating the lightest clamping force of the three used. These two failures were a loss of electrical continuity between the dice and the substrates.

Calculations indicate a maximum shear of 10,600 psi on the aluminum interconnection cones at worst-case conditions. (See Appendix III) The interconnection cones, alloy 1100 aluminum, are capable of a maximum shear strength of 9,000 psi in the annealed condition and 13,000 psi in the full hard condition; i.e., condition H-18, (1). It must be assumed, therefore, that the aluminum cones are work hardened to some extent during face bonding to sustain this worst-case calculated shear stress.

The aluminum interconnection cones are hardened to the 1/2 hard condition or greater based on their ability to resist the worst-case calculated, 10,600 psi shear. This conclusion appears reasonable due to the amount of upset of the aluminum interconnection cones experience during bonding. (Initially, the cones are 0.004 inch in diameter at the base with a height of 0.0015 inch. After bonding, they are deformed to an elliptical shape with the minor axis of 0.005 inch and major axis of 0.008 inch, the final height being about 0.00025 inch.)

The RACD program was designed to provide a range in stress levels and based on the calculations herein, the shear limit of the interconnection cones may be exceeded. (The temperature range for this investigation was -34.5 to 79.5 C, whereas the temperature range for the contracted program is -50 to 200 C.) The coefficients of expansion of the Corning 7059 glass and the silicon dice as used in this investigation are fairly close to one another; i.e., 4.6×10^{-6} in/in/C and 2.0×10^{-6} to 2.85×10^{-6} in/in/C, respectively in the temperature range of -35 to 80C, (2). However, the coefficient of expansion for Corning soda lime glass is quite different from silicon

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(1) "Metals Handbook," Vol. 1, Eighth Edition, p. 936, published by the American Society for Metals.

(2) "7059 Glass Substrates" by Corning Electronics, Corning, New York.

and it can be anticipated that interconnection bond failure will probably occur with this material. A number of the face-bonded samples made with high-expansion (soda lime) glass are expected to fail due to excessive stresses during the temperature-cycling phases. Such information will be valuable in helping to define constraints for face-bonded assemblies.

3. PROCEDURE AND RESULTS

Materials were obtained for schedule development and bonding of samples to be thermal cycle tested. The silicon dice used were 0.060 x 0.080 inch with the 1304B shorting bar interconnection aluminum metallization pattern, Figure 16. The substrates were 0.048 inch thick Corning 7059 glass with aluminum 1304B fan-out interconnection pattern.

Aluminum interconnection cones were formed and joined to the aluminum interconnection pads on the silicon dice for each die used in this investigation. These cones were 0.0040 inch in diameter and 0.0015 inch high. They were formed and joined by the Hughes, Model 2901, Flip Die and Wire Bonder with a special cone-making tip.

Three different bonding schedules were developed by face bonding dice to the substrates with the Gulton G-10 power supply. The three schedules developed for use on the test specimen were as follows:

Schedule ID	Clamping Force (grams, ±2 percent)	Power On Time (seconds, ±5 percent)	Resonance Level (volts ±0.1 volt)
I	1300	1.0	9.2
II	1100	1.0	9.6
III	1000	1.0	9.6

The test face-bonded samples for the preceding schedule development all exhibited 100-percent electrical continuity and a minimum shear strength of 300 grams.

Face bonding was then performed on 36 dice to one substrate for the thermal cycle test specimen. Twelve dice were face bonded using each of the three schedules developed.

The test specimen was checked for electrical continuity by measuring the voltage drop across each interconnection cone with a VTVM. The specimen was then subjected to four thermal cycle periods. An electrical continuity determination was performed for each interconnection cone after each thermal cycling. The four thermal cycle excursions were as follows.
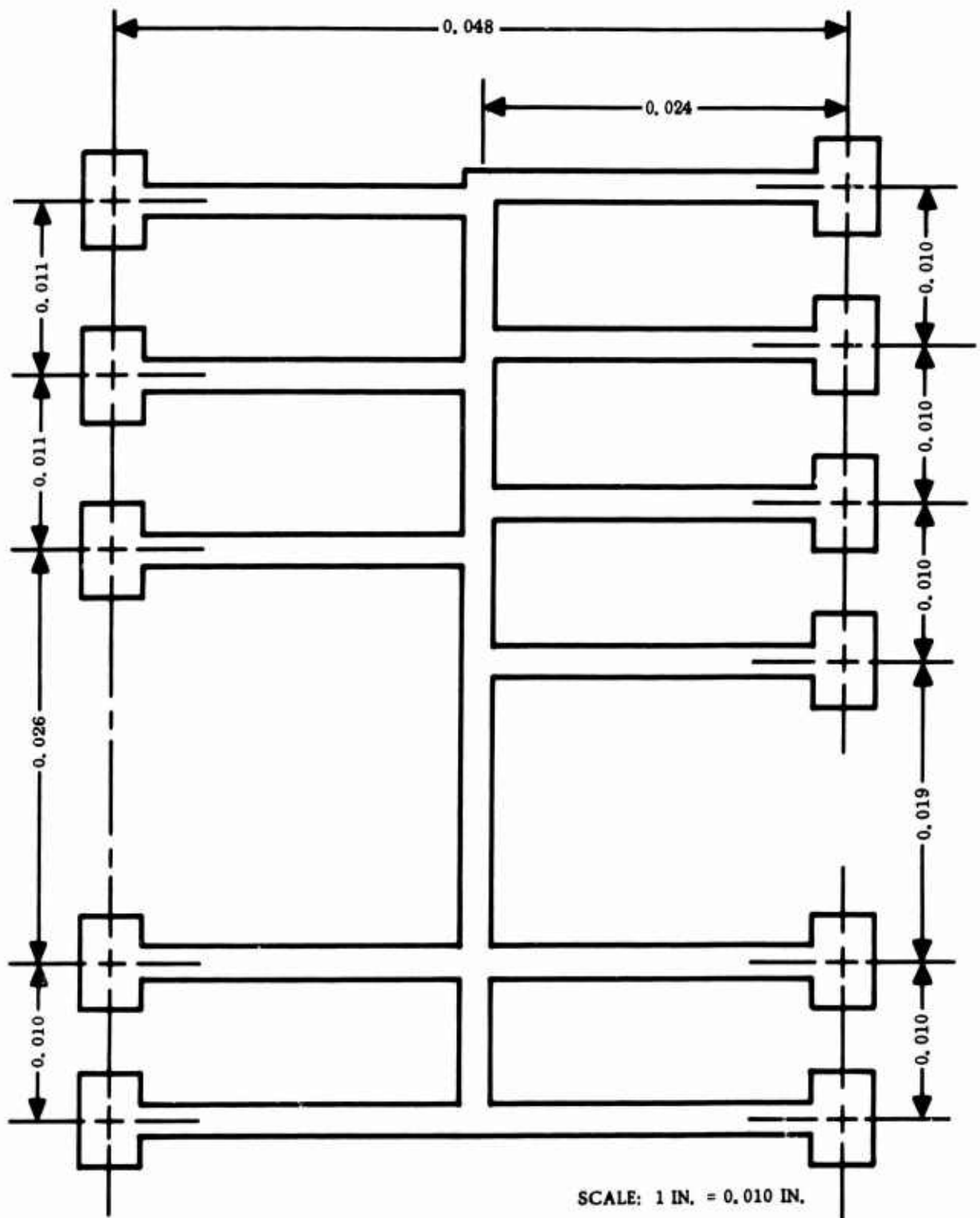
96

Figure 1.   1304B Continuity Pattern

97

First: Room Temperature[9] → (-10 → +125 F) → Room Temperature; 2 times

Second: Room Temperature → (-10 → +125 F) → Room Temperature; 8 times

Third: Room Temperature → (-30 → +175 F) → Room Temperature; 2 times

Fourth: Room Temperature → (-30 → +175 F) → Room Temperature; 8 times

One die came off of the substrate after being lightly tapped with a probe during electrical continuity testing after the second thermal cycle. Another die exhibited three open contacts after the third thermal cycle.

The remaining dice showed no significant changes after all four thermal cycle excursions.

Following cycling and electrical continuity test, the dice were shear tested to determine bond strength. The shear test results were as follows:

Strength	Grams[10]
Average	540
High	1310 (Bonding Schedule I)
Low	90 (Bonding Schedule III)

The shear strengths with respect to bonding schedule and compared to schedule development shear strengths is as follows:

Schedule No.	Number of Dice in Group	Development Samples Average Strength [10] (grams)	Test Specimen Average Strength After Thermal Cycle (grams)
I	12	682	693
II	12	541	533
III	11	333	380

---

9. The temperatures were determined ±IF

10. ±5 percent

APPENDIX III

COMPUTATION OF APPROXIMATE SHEAR STRESS
IN FACE BONDING CONES

The model for this computation is as follows:

1. For the thermal stress generated along an axis across the chip, it is assumed that two bars 0.011 inch wide, one of silicon and the other of glass, were attached at their ends. The silicon was 0.007 inches thick and the glass was 0.048 inches thick. These two bars were attached by cones 0.048 inches apart along their length. It is assumed that the stress distribution in the bar is uniform across the section. See Figure 1, Appendix II.

2. For the thermal stress generated along an axis parallel to the length of the chip, the same cross section dimensions and uniform stress distribution were assumed, but the length between the end cones is 0.059 inches.

The range of the thermal cycling tests was -30 to 175 F or -34.5 to 79.5 C. It is assumed that at 20 C the strain between the two materials was zero. The maximum temperature change occurs when the specimen is heated to +80 C. A value of T_0 = 20 C and T_1 = 80 C will be used to compute the estimated maximum thermal stress.

The coefficients of thermal expansion are:

Silicon $\qquad \alpha_1$ = 2.0 x 10^{-6} in/in/C at -35 C

$\qquad\qquad\qquad\quad$ = 2.33 x 10^{-6} in/in/C at 20 C

$\qquad\qquad\qquad\quad$ = 2.85 x 10^{-6} in/in/C at 80 C

Glass, Owens $\quad \alpha_2$ = 4.6 x 10^{-6} in/in/C, nearly constant in 0 to 300 C range.
Corning 7059

The stress in the bars attached at their ends and constrained against buckling is: (1)

$$\sigma_1 = -\ \frac{\alpha_1\, E_1\, (T_1 - T_0)\left(1 - \dfrac{\alpha_2}{\alpha_1}\right)}{1 - A_1 E_1 / A_2 E_2}$$

Subscripts: 1 refers to silicon
$\qquad\qquad\quad$ 2 refers to glass
$\qquad\qquad\quad$ E_1 = 27.3 x 10^{-6} psi $\qquad\quad A_1$ = 7.7 x 10^{-5} in.^{2}
$\qquad\qquad\quad$ E_2 = 9.8 x 10^{6} psi $\qquad\qquad A_2$ = 5.28 x 10^{-4} in.^{2}

---

(1) "Thermal Stresses," Gatewood, McGraw-Hill.

$\sigma_1 = 3465$ psi

$F = A_1 \alpha_1 = 0.267$ lb

Shear stress in a cone:

The cross section of the cones is nearly elliptical, with major and minor diameters of 0.008 and 0.005 inches respectively. The area of an ellipse is $A_c = \pi ab$.
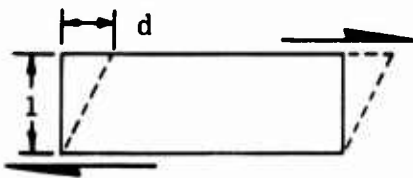
$A_c = \pi \times 0.004 \times 0.0025 = 3.14 \times 10^{-5}$ in^2

The shear stress across the cone is:

$$\sigma_S = \frac{0.267}{3.14 \times 10^{-5}} = 8500 \text{ psi}$$

Relaxation Effect of Deformation of Cone:

$$d = \frac{\sigma_s \, 1}{E_s}$$

E_s for 1100 Al alloy is 3.75×10^6 psi.

Transverse Shear:

$$d = \frac{8500 \times 5 \times 10^{-4}}{3.75 \times 10^6} = 1.13 \times 10^{-6} \text{ inches}$$

Deflection of the silicon:

$$d_{si} = \frac{3465 \times 0.048}{27.3 \times 10^{-6}} = 6.1 \times 10^{-6} \text{ in}$$

$$\sigma_2 = \frac{0.267}{5.28 \times 10^{-4}} = 5.06 \times 10^2 \text{ psi}$$

$$dg = \frac{506 \times 0.048}{9.8 \times 10^6} = 2.48 \times 10^{-6} \text{ inches shortening of the glass.}$$

$d_{si} + dg = 8.58$ microinches deflection in silicon and glass if it is assumed that the aluminum cone is rigid. If the aluminum is allowed to relax, then, as a first iteration,

$$\frac{1.13}{8.58} = 0.132 \text{ fractional relaxation.}$$

Therefore, the transverse shear stress in the cone is

$$\sigma_S = 8500 \ (1 - 0.132) = 7380 \text{ psi.}$$

Longitudinal Shear:

The shear stress (before relaxation) in the direction parallel to the longitudinal axis is the same as before:

$$\sigma_S = 8500 \text{ psi.}$$

Relaxation effect is computed as follows:

Total deformation of glass and silicon is:

$$8.58 \times \frac{0.059}{0.048} = 10.52 \text{ microinches}$$

$$\frac{1.13}{10.52} = 0.107 \text{ fractional relaxation.}$$

$$\sigma_S = 8500 \ (1 - 0.107) = 7600 \text{ psi.}$$

Biaxial or resultant shear stress:

$$\sigma_{SR} = \sqrt{(7380)^2 + (7600)^2} = 10600 \text{ psi.}$$

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13. ABSTRACT

Phase One of this program was concerned with the effect of ultrasonic bonding energy on the oxide coating of integrated circuit chips. The results of this study indicate that a low level of oxide defects is caused by ultrasonic face bonding.

Phase Two was to experimentally determine the optimum face-bonded assembly design. The "practical best" design was found to be that which employed a biaxial bonding pattern, a 7059 glass substrate and aluminum projections with an as-bonded height of 2 to 3 x 10^{-4} inches.

Phase Three was to fabricate and test a number of the "practical best" assemblies. The results showed that there was little or no effect of thermally induced mechanical stress, and that electrical continuity was maintained throughout the twenty thermal cycles.

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